

Compal confidential BAP00 schematic document

Sky Lake-H platform with nVIDIA N17E-G1
Kaby Lake-H platform with nVIDIA N17E-G1
Kaby Lake-H platform with nVIDIA N17P-G0-B/N17P-G1-B
Rev: 1.0(A00) PVT
2016/09/05(BOM 2016/09/06)

@ : Nopop component
EMI@ / @EMI@ : EMI pop / unpop part
ESD@ / @ESD@ : ESD pop / unpop part
RF@ / @RF@ : RF pop / unpop part
CONN@ : Connector component
CMC@ : CMC debug
TBT@ : Thunderbolt
PD@ : Thunderbolt PD
SKL@ : Sky lake CPU
KBL@ : Kaby lake CPU
N17E@ : N17E-G1
N17P@ : N17P-G1-B / N17P-G0-B

PR8211 PR8211
34.8K 0402_1% 30K 0402_1%
SAMSUNG@ MICRON@

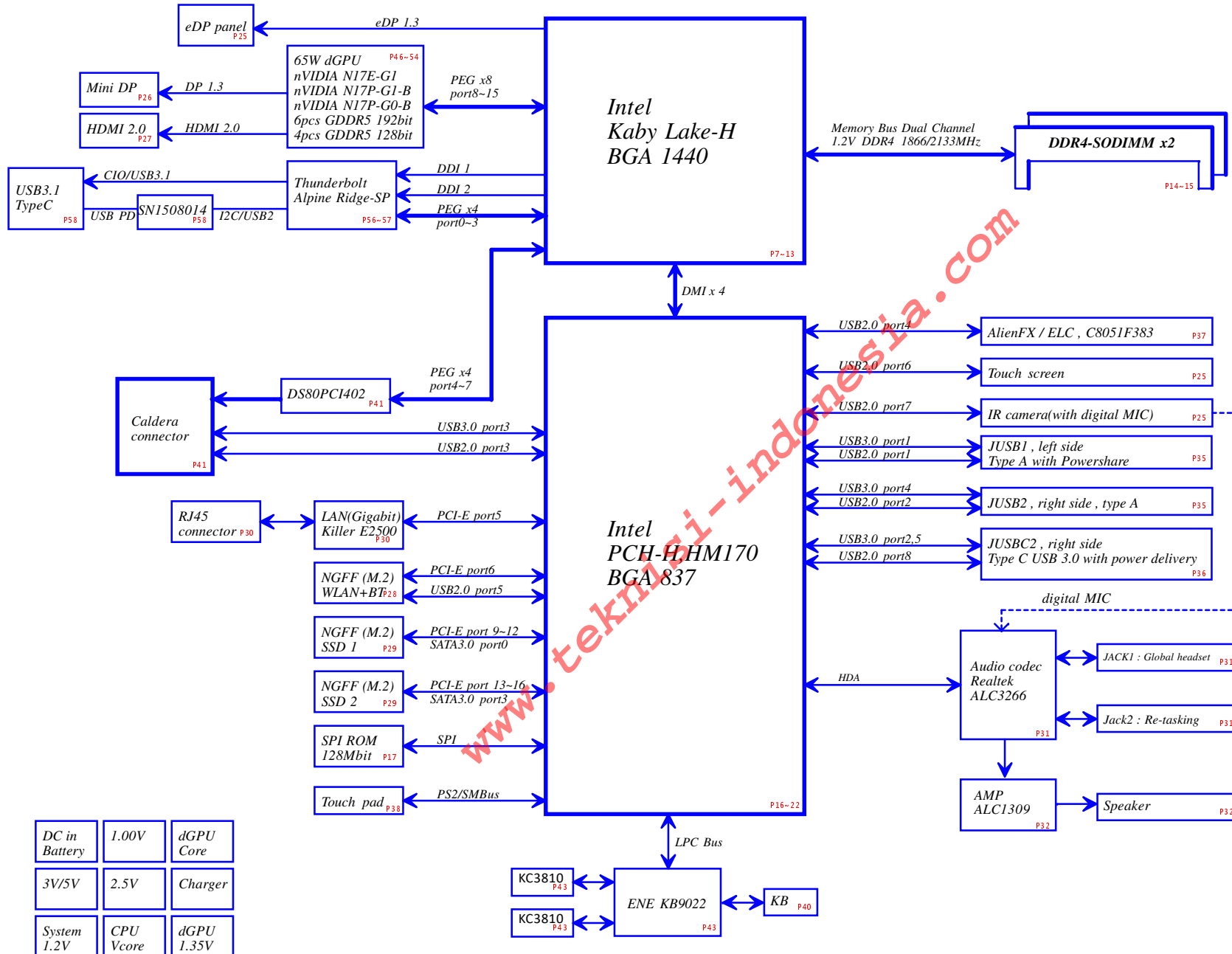
PR8215 PR8215
52.3K 0402_1% 68.1K 0402_1%
SAMSUNG@ MICRON@

DAX PCB
DAZ18F00100
PCB 18F LA-B752P REV0 M/B 8
R1@

DAX PCB
DAZ18F00101
PCB 18F LA-B752P REV0 M/B 8
R3@

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				Date Wednesday, September 07, 2016	Rev 0.4
				Sheet 1	of 80

Block Diagram



Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA45- 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xFF
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCGT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS	DDR4 +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PCH_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+PEX_VDD	+1.0VS power rail for GPU	ON	OFF	OFF
+1.35VS_VGA	+1.35~1.55VS power rail for GPU	ON	OFF	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+VCCST	+1.0V power rail for CPU	ON	ON	OFF
+VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3V_PCH	+3VALW power for PCH DSW rails	ON	ON	ON*
+LAN_IO	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1V8_AON	+1.8VS power rail for GPU	ON	OFF	OFF
+3V3_SYS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+RTC_CELL	RTC power	ON	ON	ON
+VCCSA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

PCH-H, HM170

HSIO	USB3	PCIe	SATA3	Function
1	1			JUSB1,type A
2	2			JUSB3,type C
3	3			Caldera
4	4			JUSB2,type A
5	5			JUSB3,type C
6	6			
7	7	1		
8	8	2		
9	9	3		
10	10	4		
11		5		LAN
12		6		WLAN
13		7		
14		8		
15		9	0	JSSD1 M.2 2280 SATA PCIe x4
16		10	1	
17		11		
18		12		JSSD2 M.2 2280 SATA PCIe x4
19		13	0	
20		14	1	
21		15	2	
22		16	3	

USB2	Function
1	JUSB1(Powershare)
2	JUSB2
3	Caldera
4	ELC
5	Bluetooth
6	Touch screen
7	Camera
8	JUSB3
9	
10	
11	
12	
13	
14	

Board ID TABLE

ID	SKL	KBL
0	EVT	
1	DVT1	EVT
2	DVT1.1	
3	DVT2	
4	GC6	
5	MP	
6		DVT1
7		DVT2
8		DVT2.1/GC6
9		MP

Part No.	Name	BOM
431A3131L01	SKL I5 G1 DIS 6G	SKL@, N17E@ ,TBT@, PD@, CMC@, EMI@, ESD@, RF@, CONN@
431A3131L02	SKL I7 G1 DIS 6G	SKL@, N17E@ ,TBT@, PD@, CMC@, EMI@, ESD@, RF@, CONN@
431A3131L03	KBL I5 G1 DIS	KBL@, N17E@ ,TBT@, PD@, CMC@, EMI@, ESD@, RF@, CONN@
431A3131L04	KBL I7 G1 DIS	KBL@, N17E@ ,TBT@, PD@, CMC@, EMI@, ESD@, RF@, CONN@

Symbol Note :

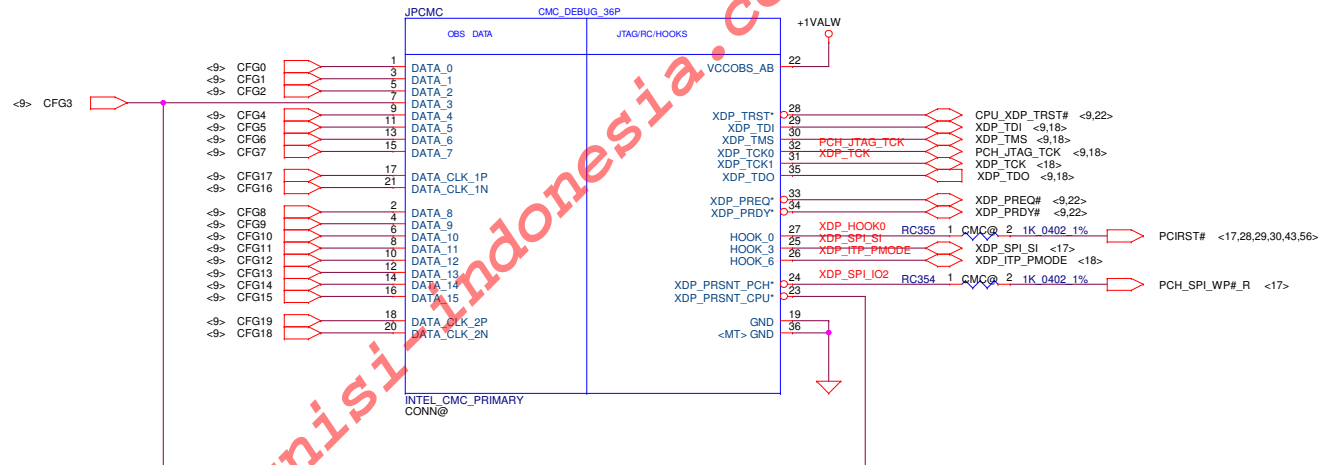
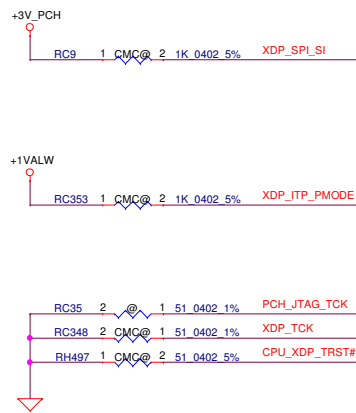


Digital Ground



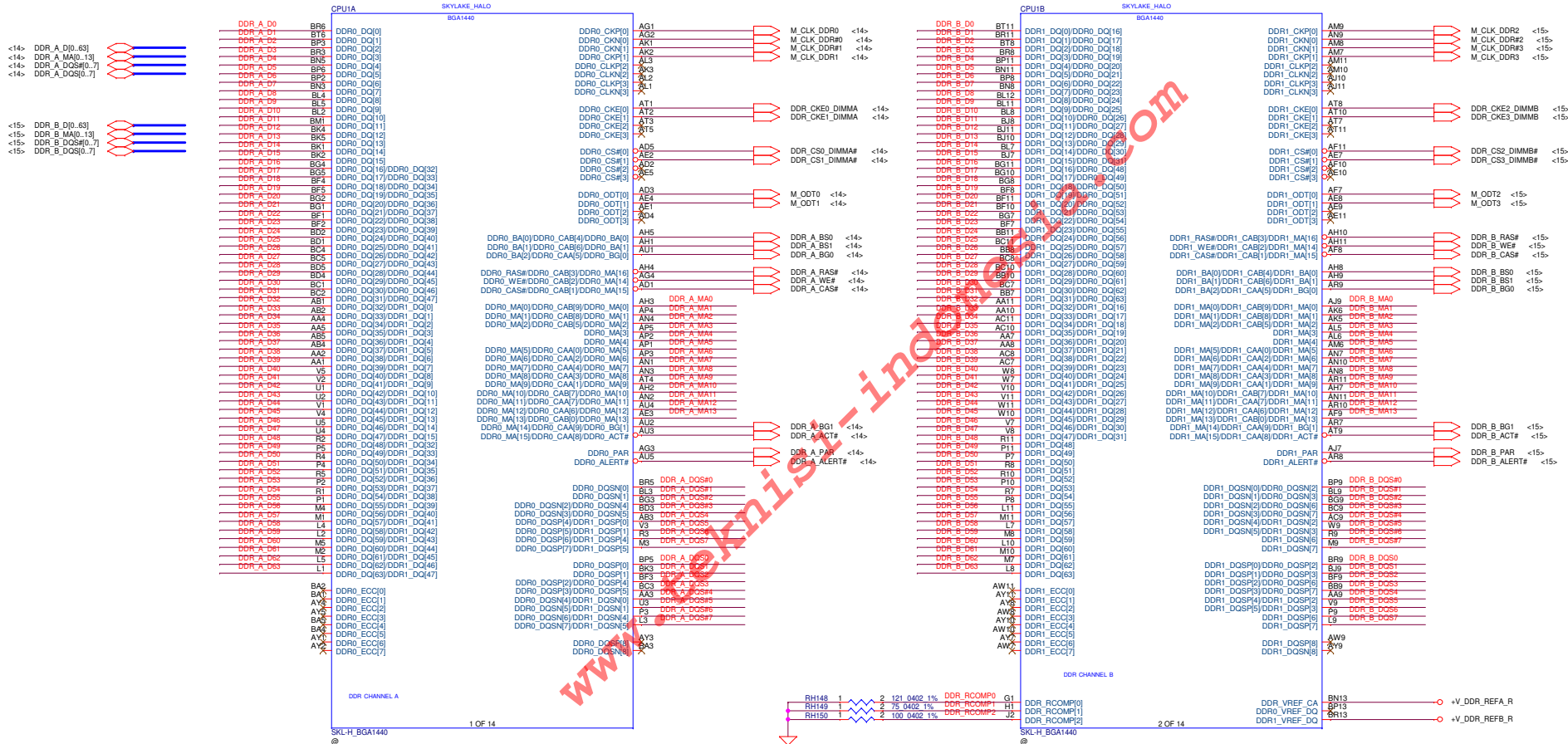
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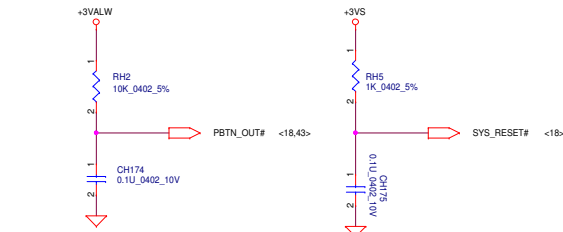
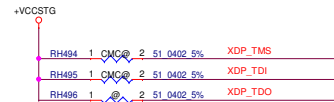
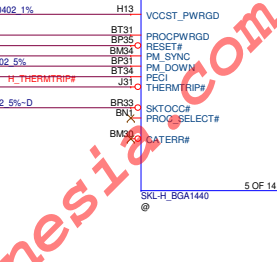
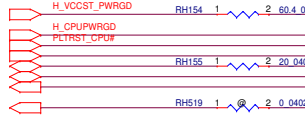
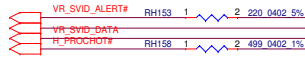
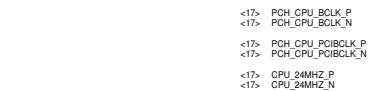
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				LA-D581P
				Rev 0.4
				Date: Wednesday, September 07, 2016
				Sheet 4 of 80

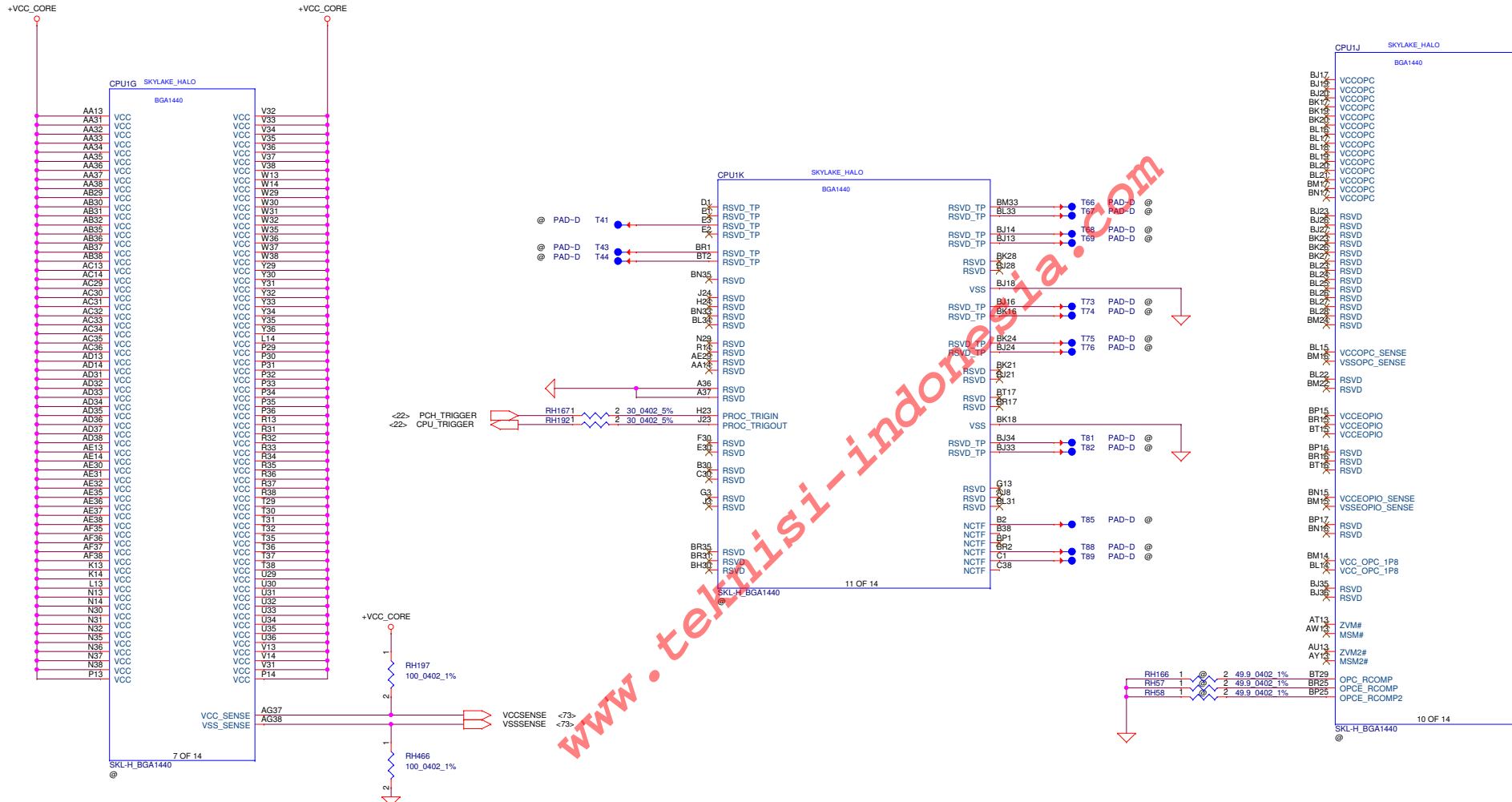


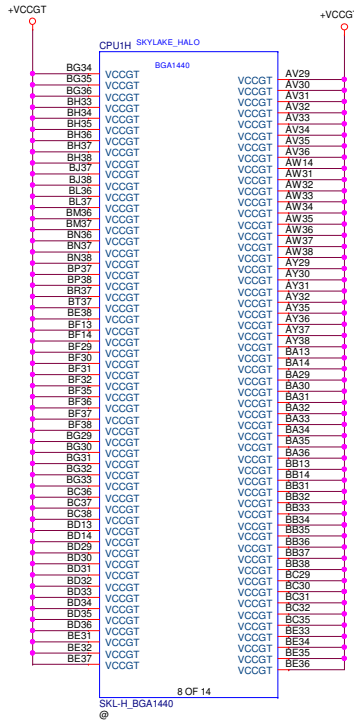
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				LA-D581P		
				0.4		
				Date: Wednesday, September 07, 2016		
				Sheet 6 of 80		

Interleave



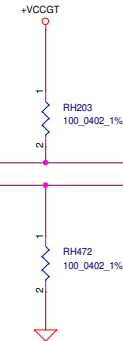




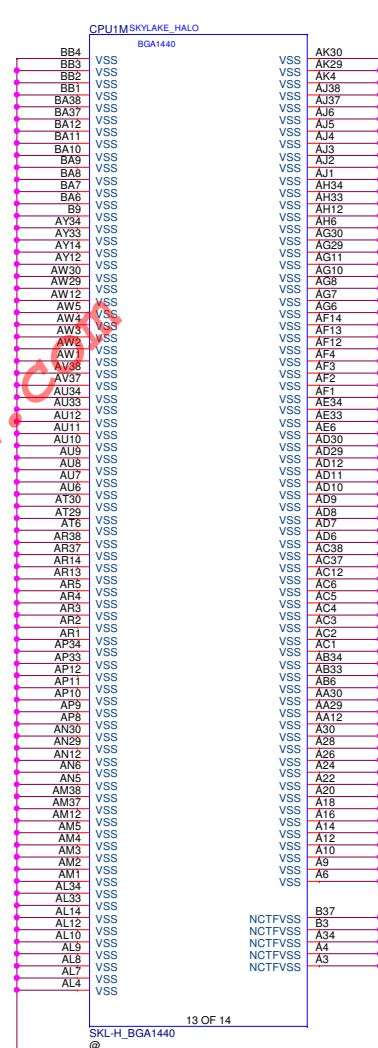
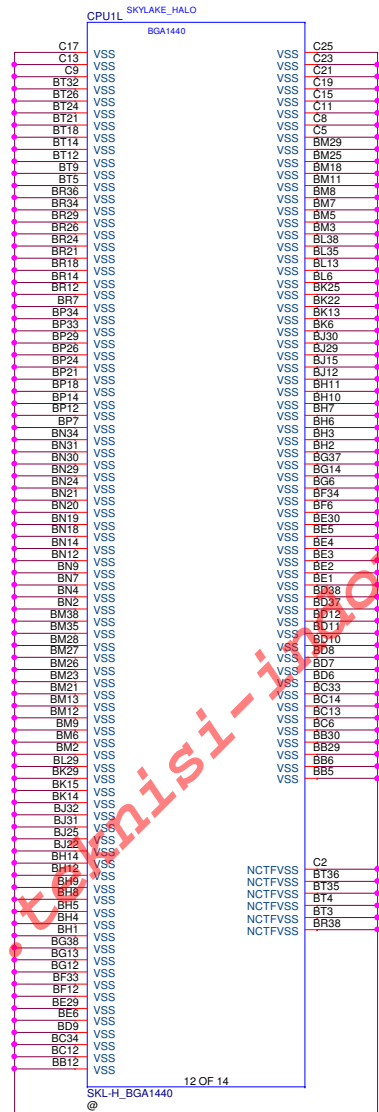
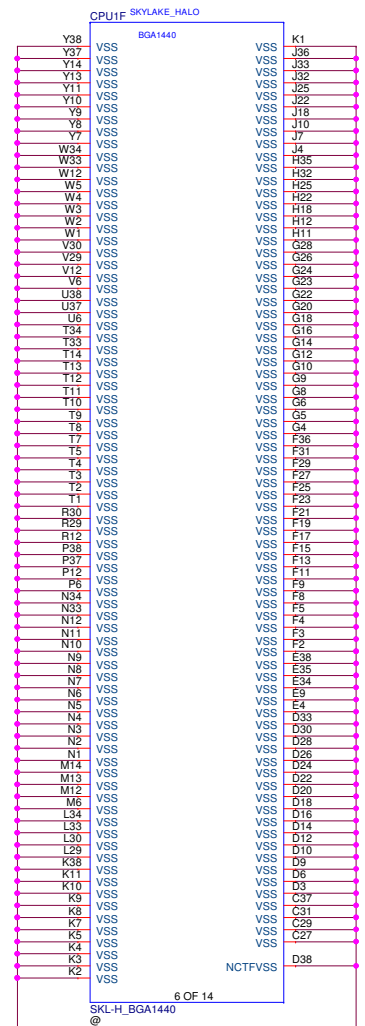


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VSSGTX_SENSE AH35
VSSGT_SENSE AH37
VCCGTX_SENSE AH36

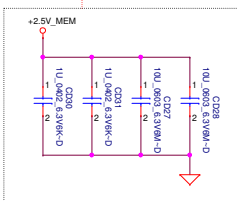
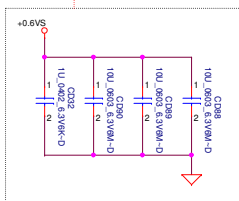
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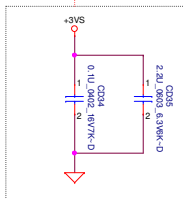
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Size	Document	Number	Rev	0.4	
Date:		Wednesday, September 07, 2016		Sheet	12 of 80



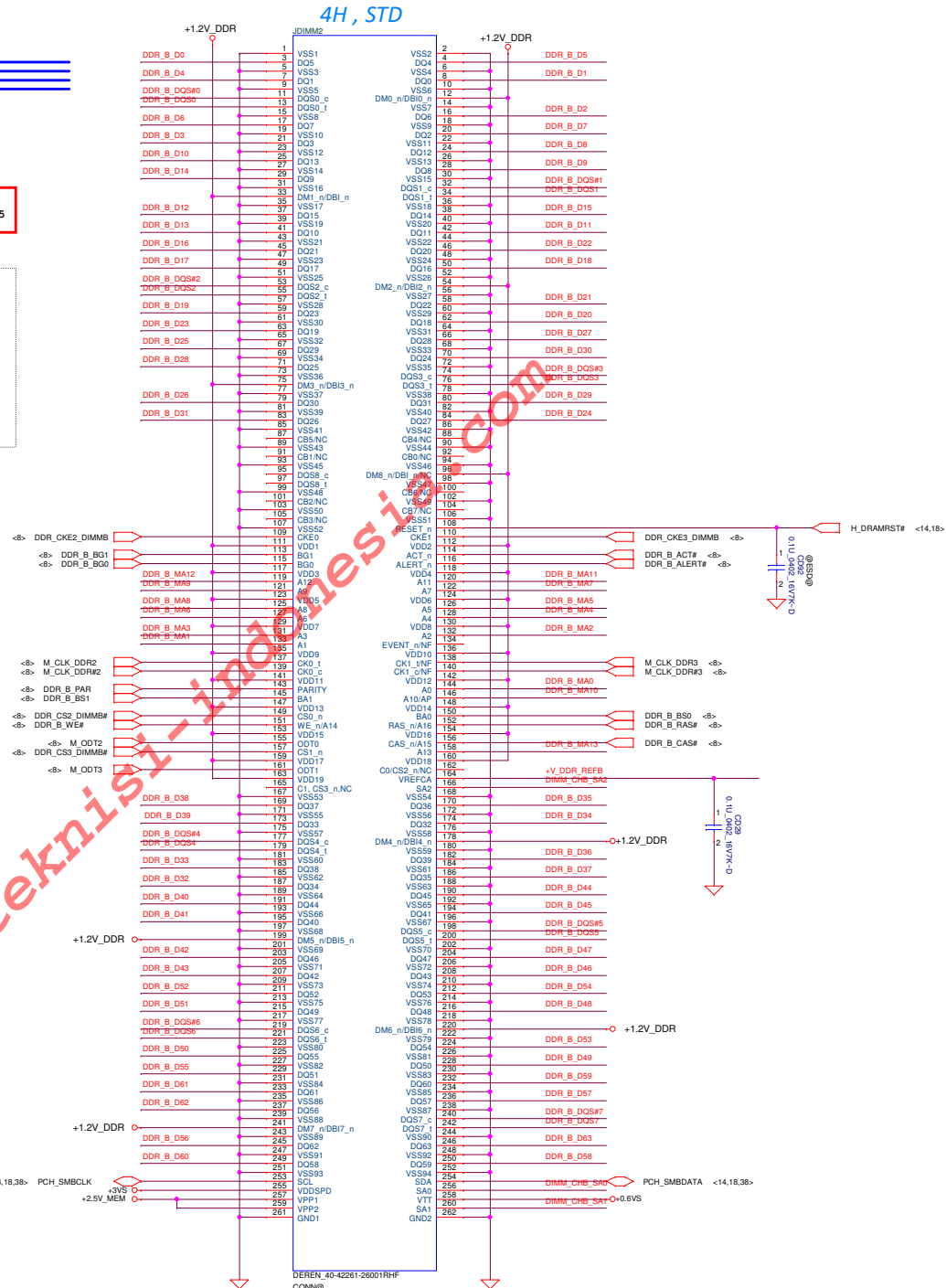
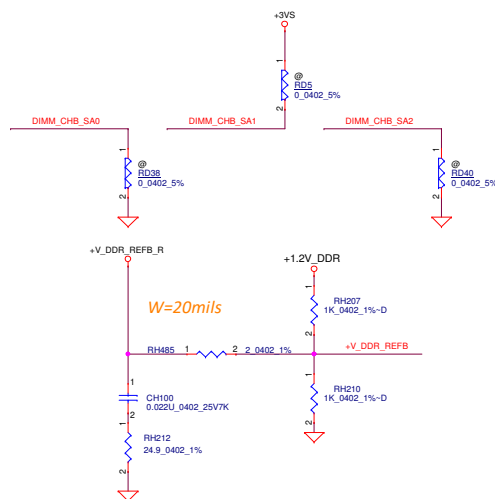
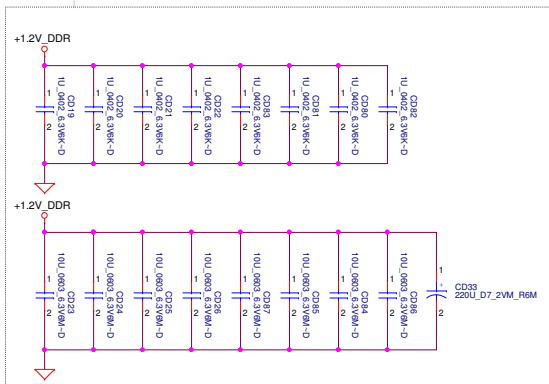
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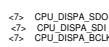
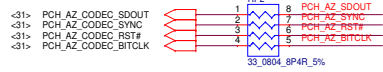
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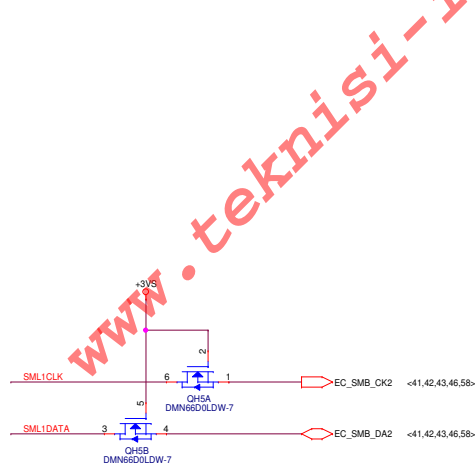
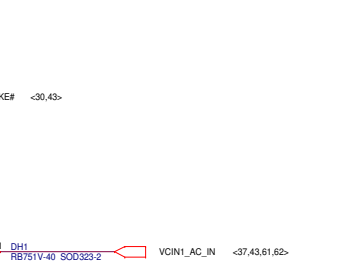
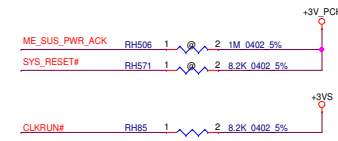
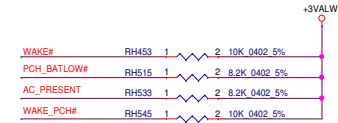
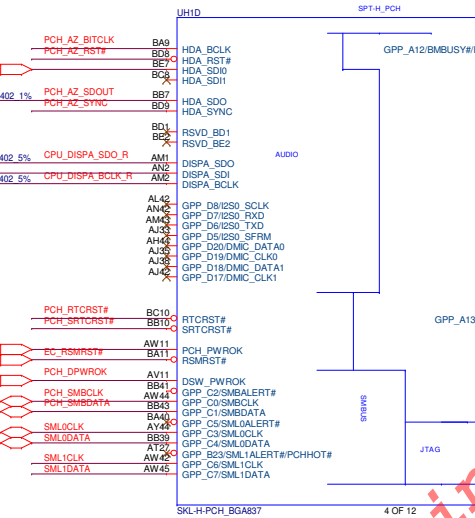
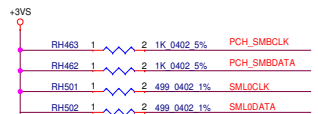
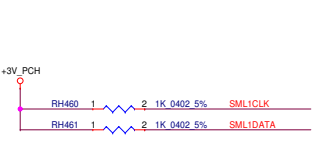
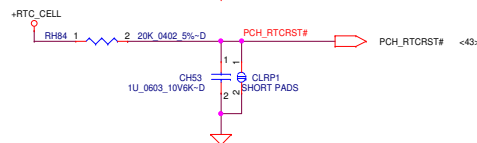
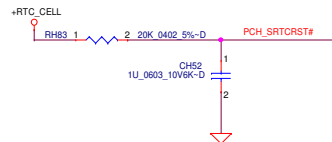
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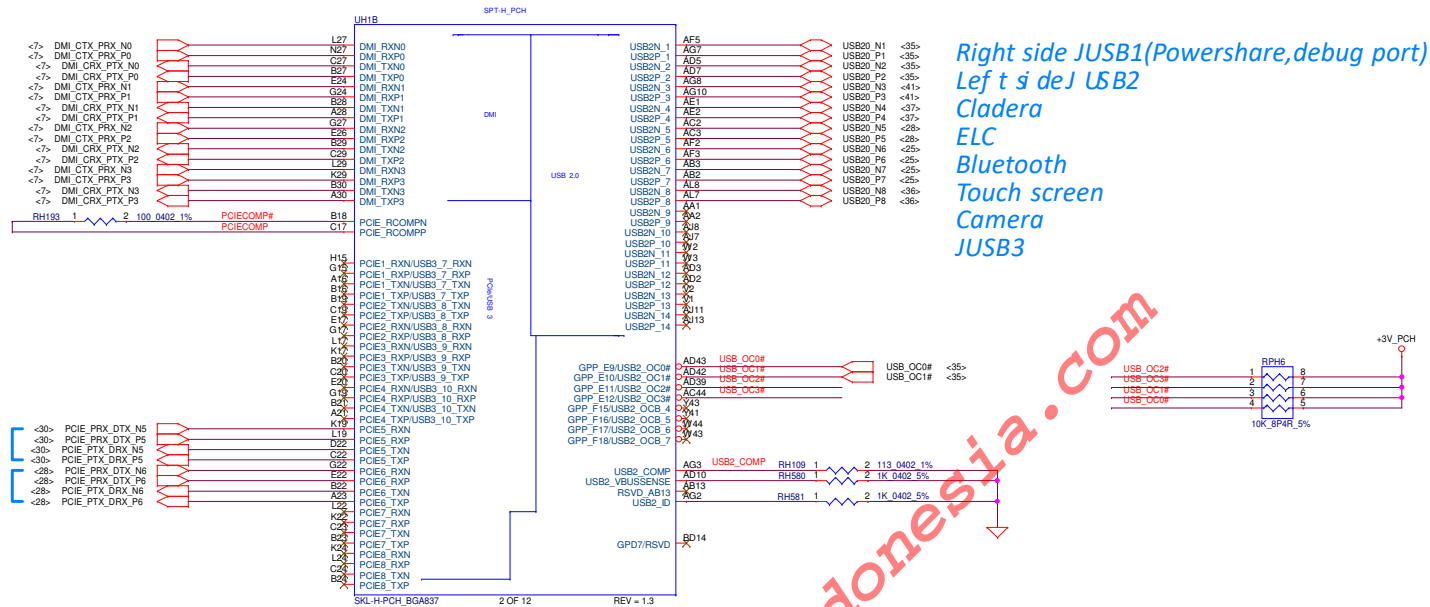
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			LA-DS51P	
Date:	2015/09/18	Sheet	15	of 80



PCH to DDR, XDP, FFS



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Issued Date	2015/09/18	Deciphered Date
2016/09/18		
Title		PCH (3/7) PM,HDA,SMB,JTAG
Size	Document Number	LA-D581P
Date	Wednesday, September 07, 2016	Sheet 18 of 80



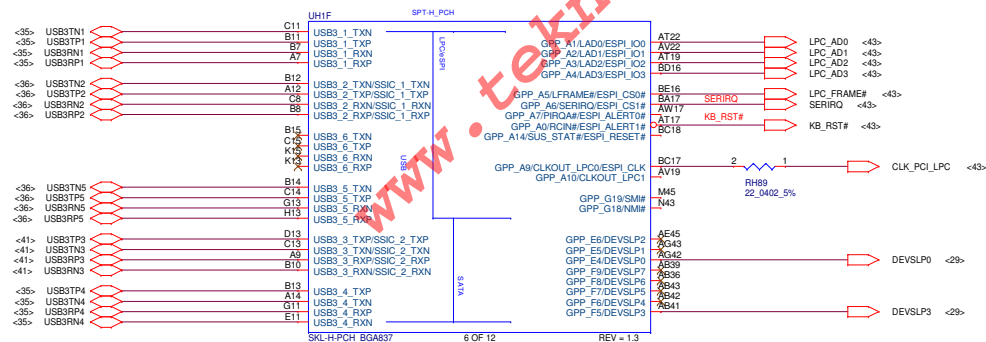
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Left side JUSB3

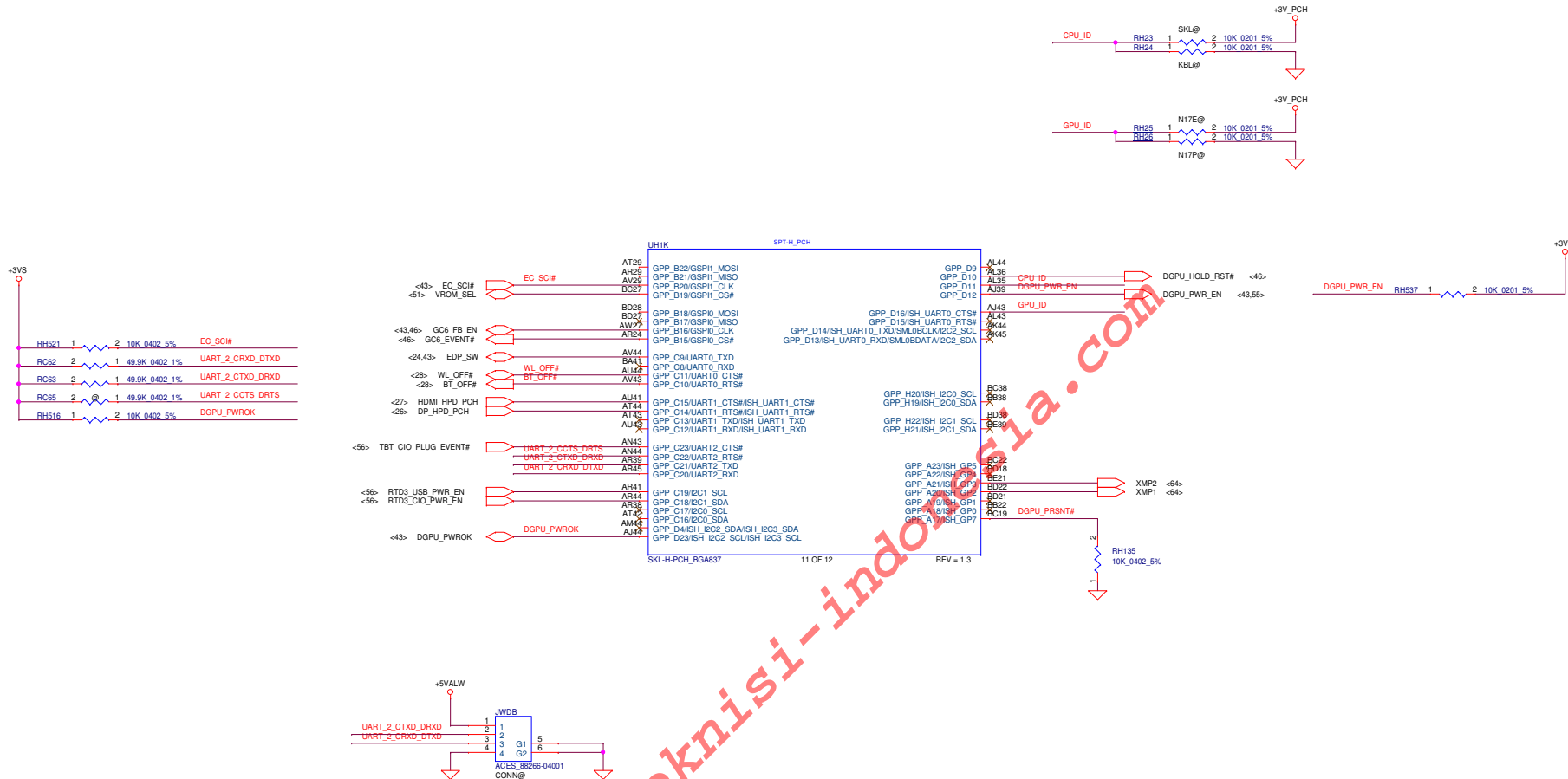
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Caldera

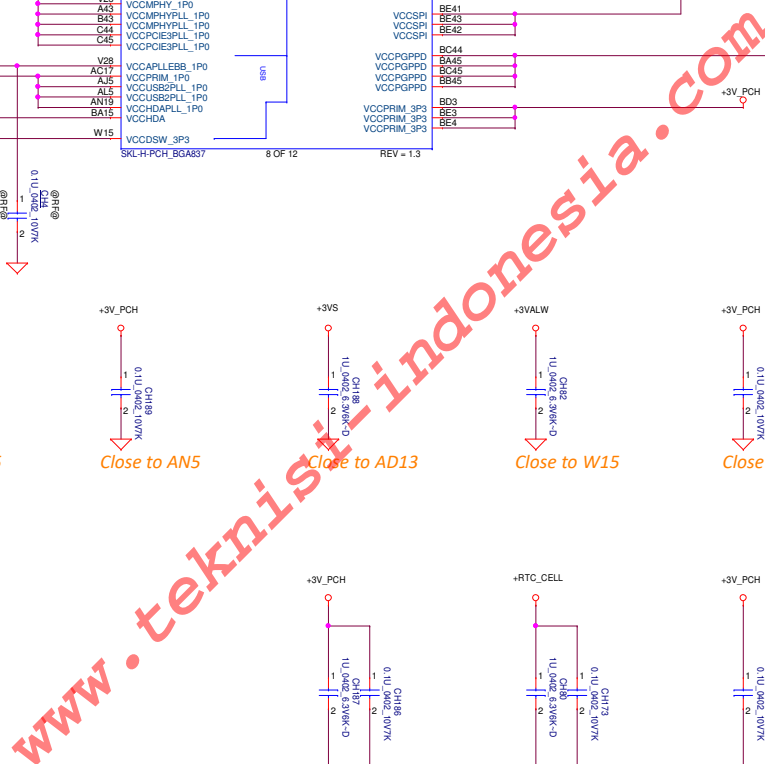
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				Size Document Number
				LA-D581P
				Rev 0.4
				Date: Wednesday, September 07, 2016
				Sheet 19 of 80



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				Size Document Number
				LA-D581P
				Rev 0.4
				Date: Wednesday, September 07, 2016
				Sheet 20 of 80



+3V_PCH

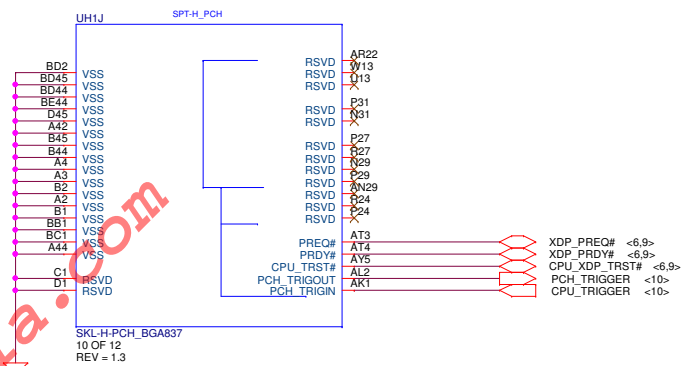
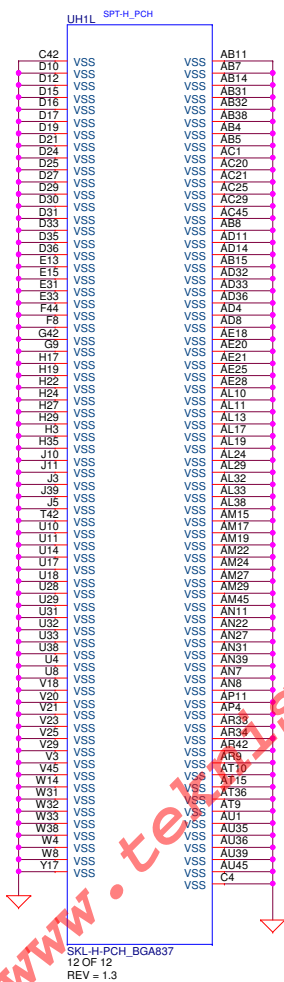
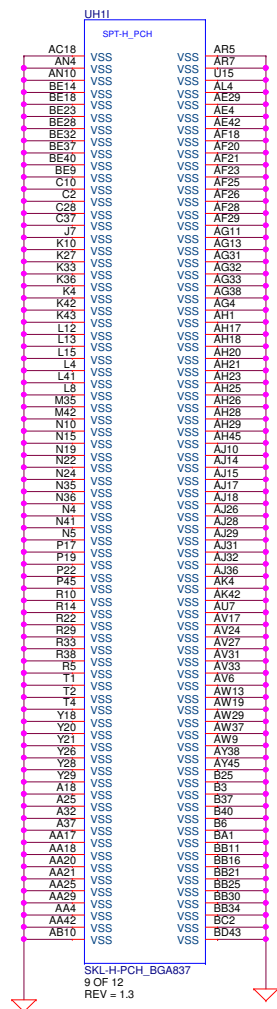
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CH192

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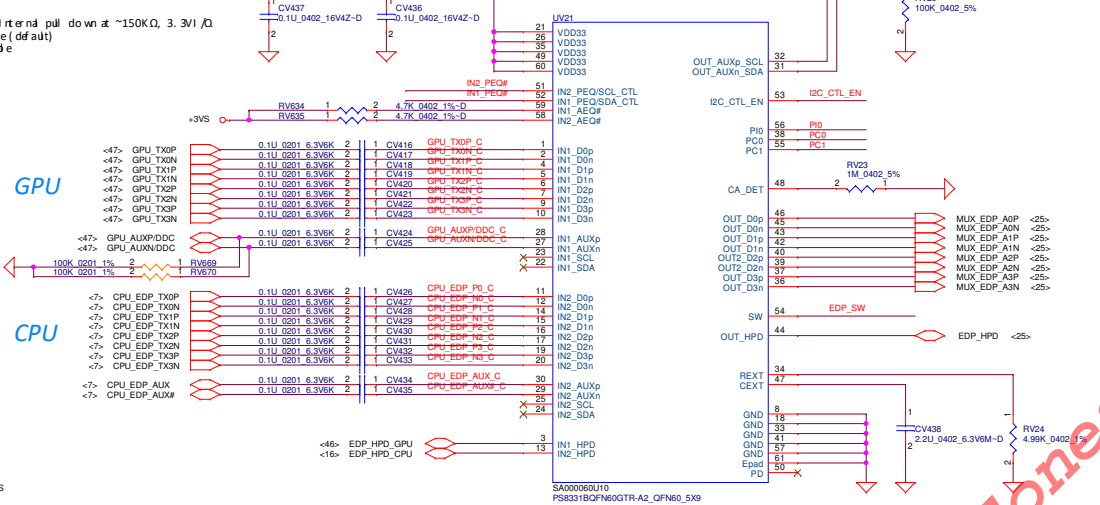
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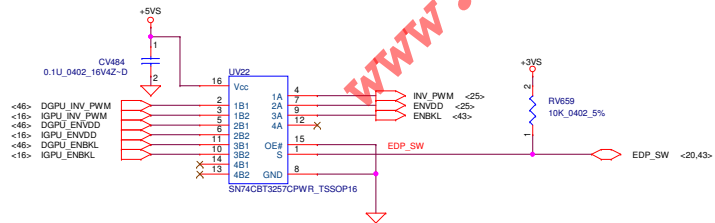


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						Rev 0.4	

IN1_AEQ#, IN2_AEQ#
Automatic EQ disable internal pull down at ~150KΩ, 3.3V / 0
L: Automatic EQ enable (default)
H: Automatic EQ disable



IN1_PEQ#, IN2_PEQ#
Programmable input equalization levels internal pull down at ~150KΩ, 3.3V / 0
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2



S1	OE	output	function
L	L	A=B1	DGPU
H	L	A=B2	IGPU
X	H		

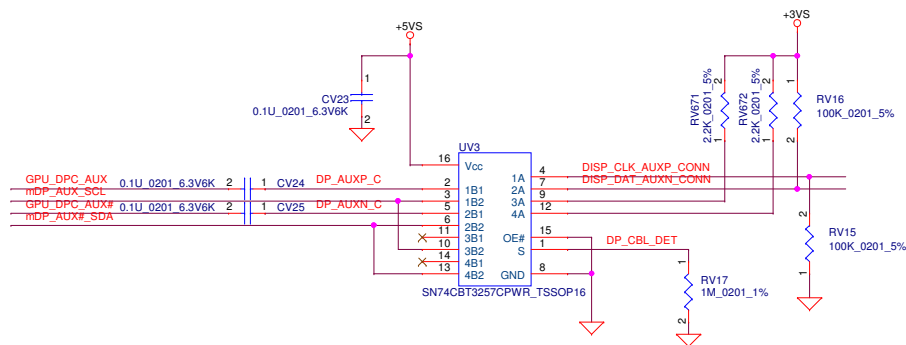
I2C_CTL_EN
I2C Control Enable; internal pull down at ~150KΩ, 3.3V / 0
L: Pin control mode is selected
H: I2C control is selected with default address 0x66/67
M: I2C control is selected with alternative address 0x08/09

PI0
Auto test enable; internal pull down at ~150KΩ, 3.3V / 0
L: Auto test disable & input of offset cancellation enable (default)
H: Auto test enable & input of offset cancellation enable
M: Auto test disable & input of offset cancellation disable

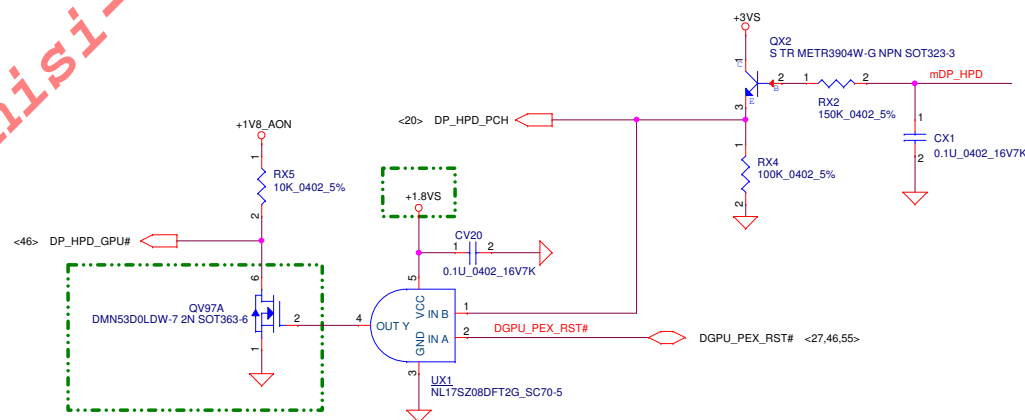
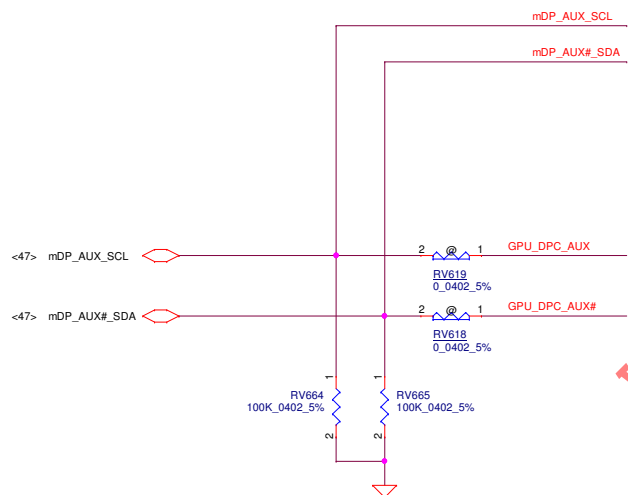
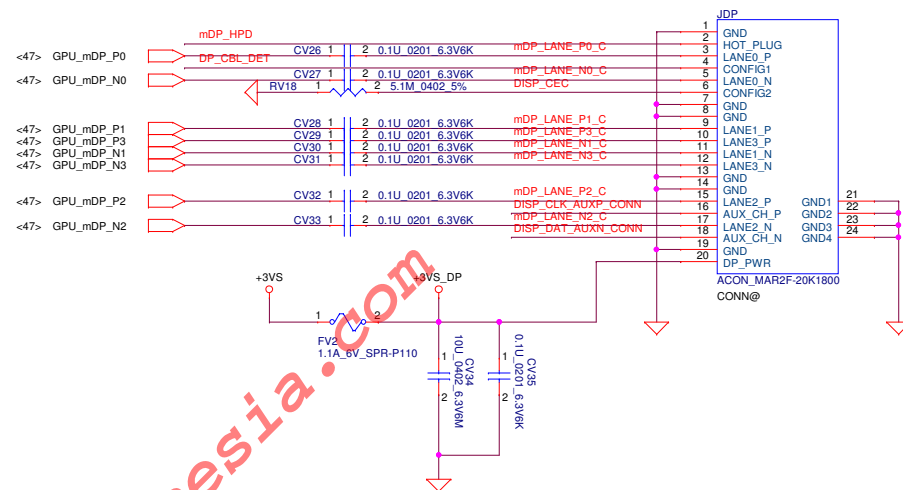
PC0
AUX interception disable or Port y (y = 1, 2) internal pull down at ~150KΩ, 3.3V / 0
L: AUX interception enable driver configuration is set by link training (default)
H: AUX interception disable driver output with fixed 50 Ohm and 0dB
M: AUX interception disable driver output with fixed 40 Ohm and 0dB

PC1
Output swing adjustment for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V / 0
L: default
H: +20%
M: -16.7%

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Issued Date	2015/09/18	Deciphered Date	2016/09/18	Title	eDP MUX PS8331B
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				Customer	LA-D581P
				Date:	Wednesday, September 07, 2016
				Sheet	24 of 80
				Rev	0.4



Function	S	OE#
mini DP cable	L	L
mini DP dongle	H	L



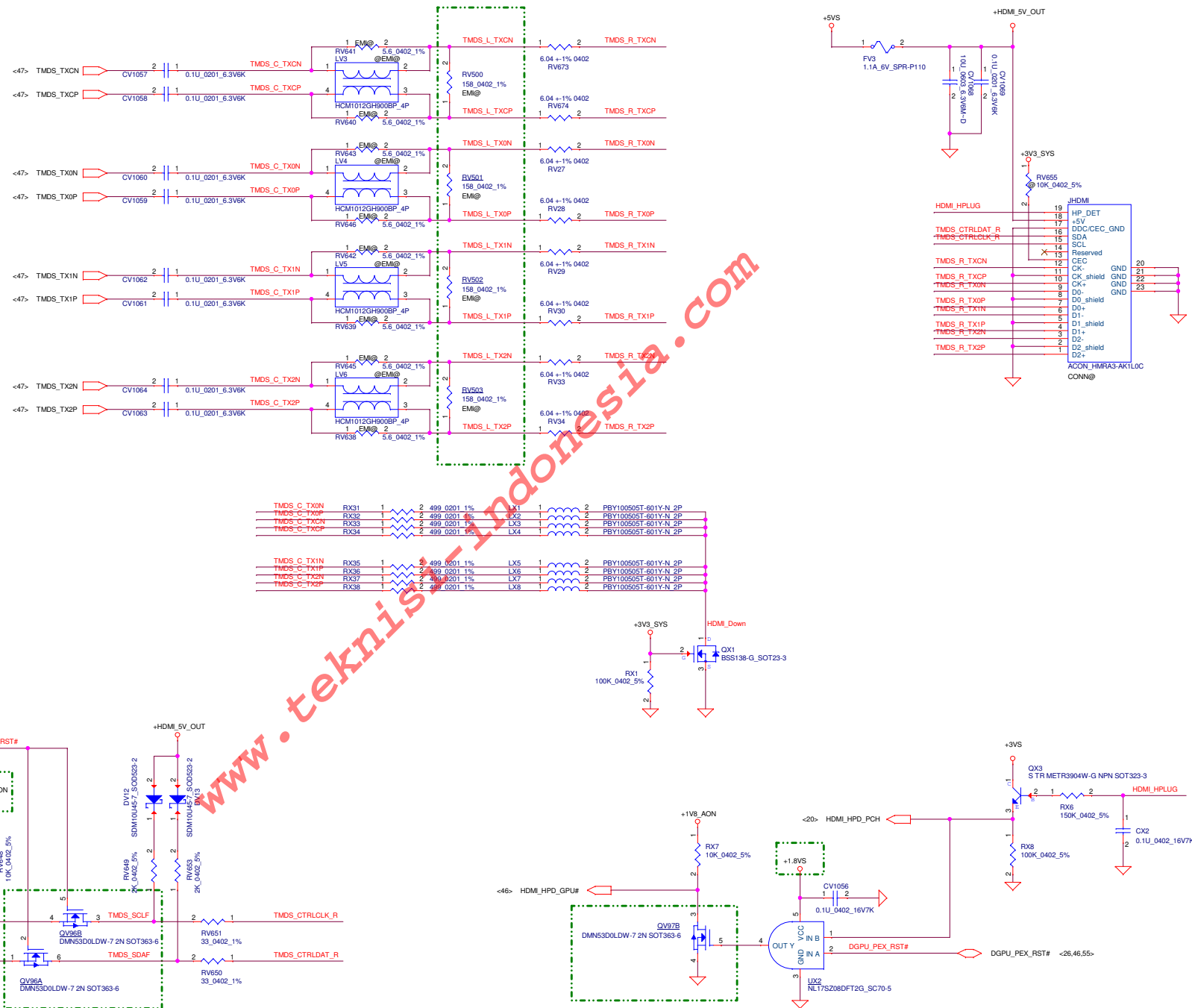
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				Date:	Wednesday, September 07, 2016
				Sheet	26 of 80

Compal Electronics, Inc.

Mini DP

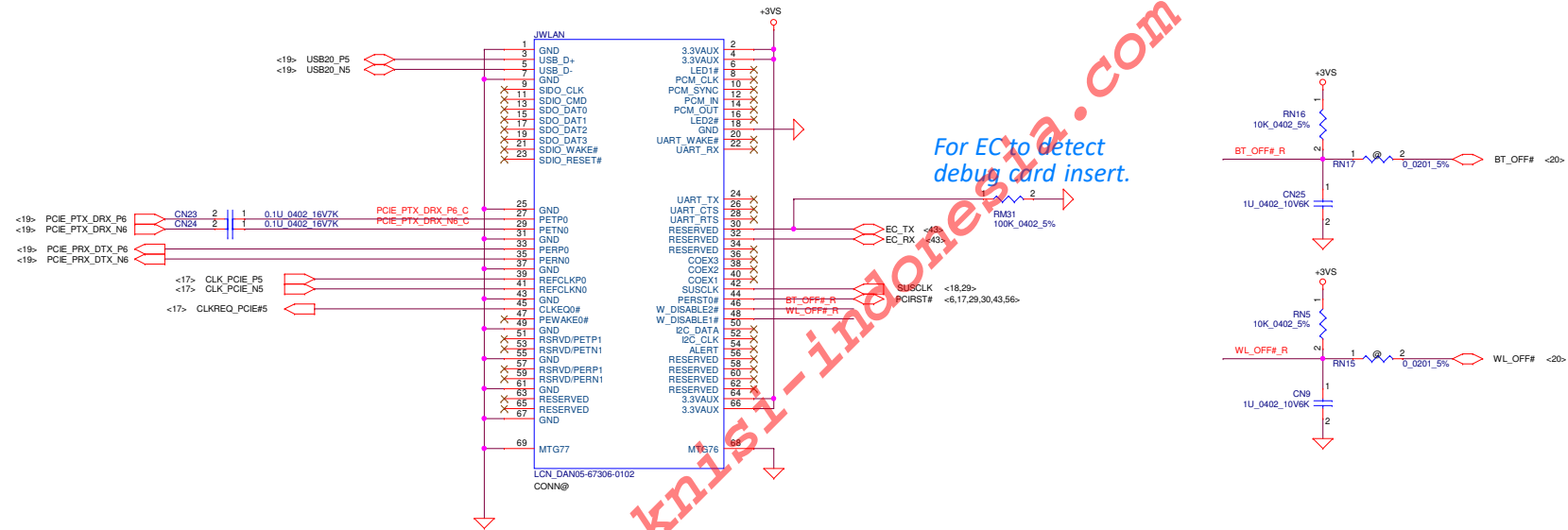
Rev 0.4

To GPU

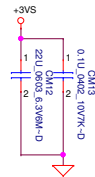


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					HDMI
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Size		Document Number			Rev
Custom		LA-581P			0.4
Date:		Wednesday, September 07, 2016		Sheet	27 of 80

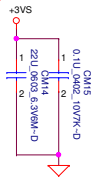
M.2 2230 slot(type E)



closed to pin 2, 4



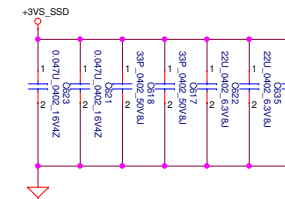
closed to pin 64, 66



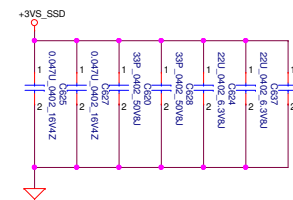
WLAN power control



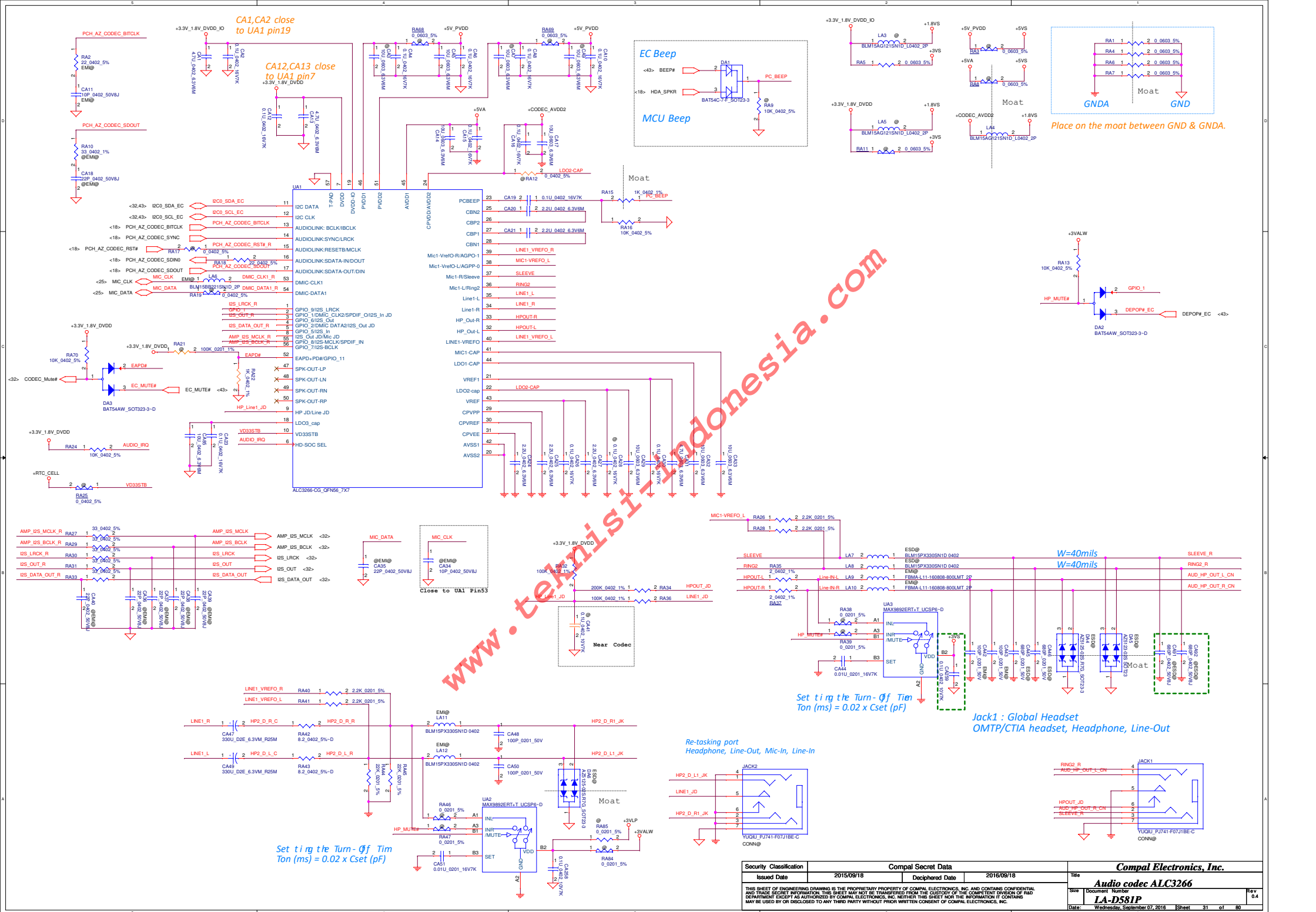
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Issued Date	2015/09/18	Deciphered Date	2016/09/18	Title	NGFF WLAN/BT
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					LA-D581P
				Date:	Wednesday, September 07, 2016
				Sheet	28 of 80
				Rev	0.4

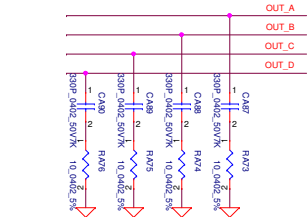
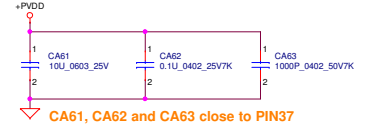
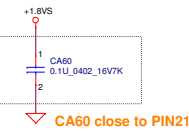
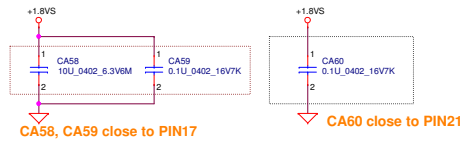
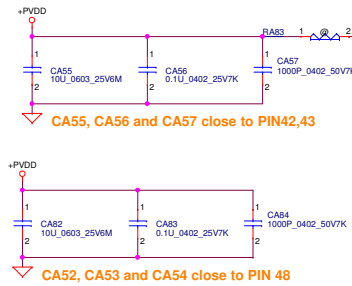
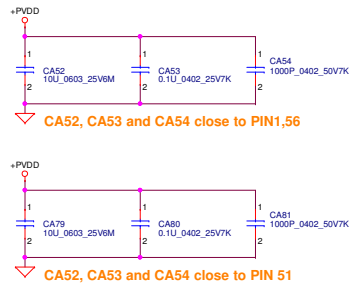
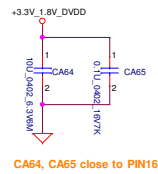
[illegible]

Pin connection diagram for the LCN_DAN05-67406-0103 connector. The diagram shows a 57-pin connector on the left and a 57-pin connector on the right. The left connector pins are labeled: 35 PERp1, 36 PETn1, 37 PETp1, 38 GND, 41 PERp0/SATA-B+, 43 PERp0/SATA-B-, 45 GND, 47 PETp0/SATA-A+, 49 PETp0/SATA-A-, 51 GND, 53 REFCLKN, 55 REFCLKP, 57 GND. The right connector pins are labeled: 32 NC, 33 NC, 34 NC, 35 NC, 36 NC, 37 NC, 38 DEVSLP, 39 NC, 40 NC, 41 NC, 42 NC, 43 NC, 44 NC, 45 NC, 46 NC, 47 NC, 48 NC, 49 PERST#, 50 CLKREQ#, 51 PERAWAKE#, 52 NC, 53 NC, 54 NC, 55 NC, 56 NC, 57 NC. The diagram shows connections for DEVSLP3 <19>, CLKREQ_PCIE#2 <17>, SUSCLK, and SUSCLK. A watermark 'www.1000pin.com' is visible across the diagram.



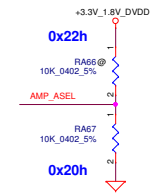
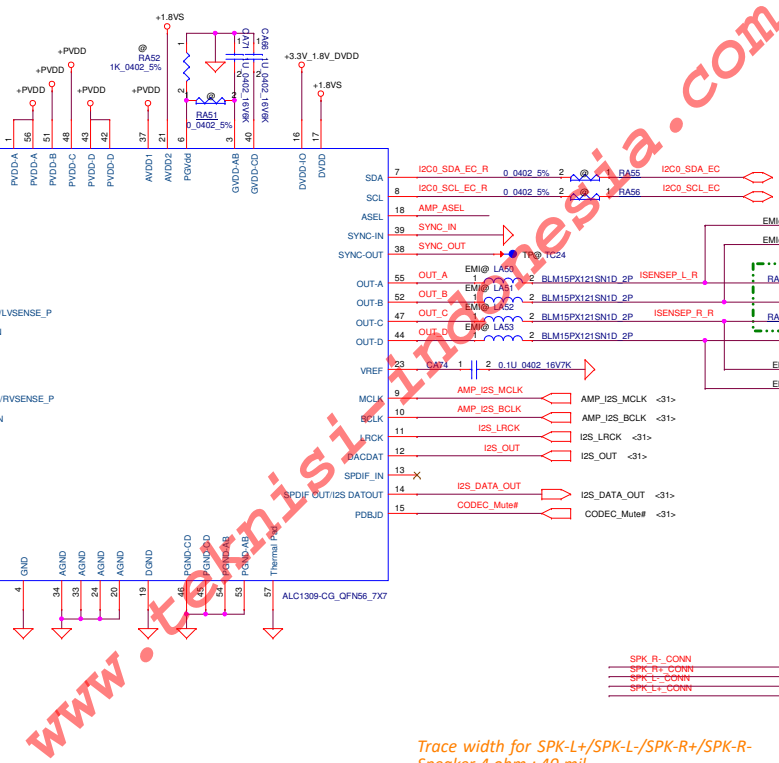
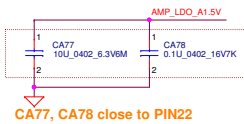
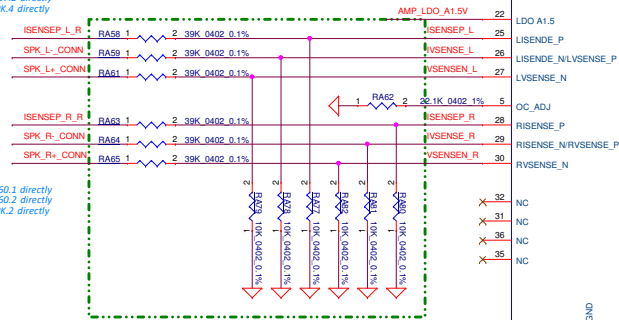
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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					LA-D581P
				Date:	Wednesday, September 07, 2016
				Sheet	29 of 80





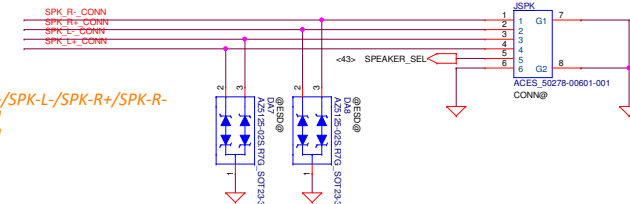
RA58.1 should from RA57.1 directly
RA59.1 should from RA57.2 directly
RA61.1 should from JSPK.4 directly

RA63.1 should from RA60.1 directly
RA64.1 should from RA60.2 directly
RA65.1 should from JSPK.2 directly

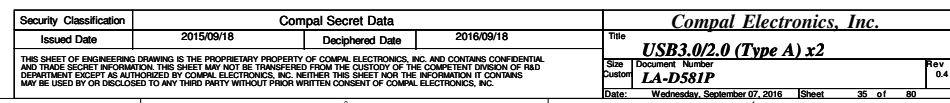


Int. Speaker Conn.

40 mils = For 4 ohm 3W Speaker
Close to UA1 Pin42,43,44,45

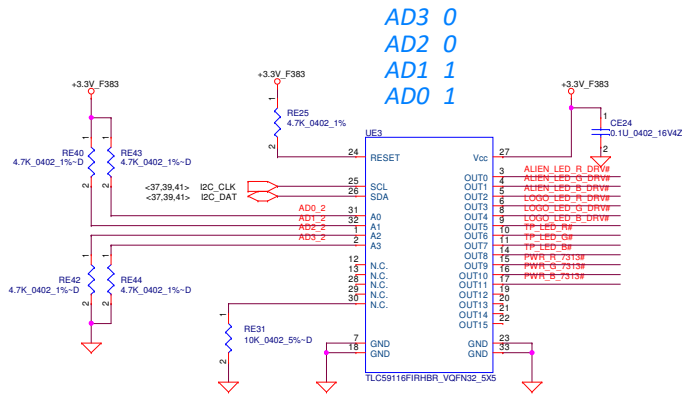


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Size	Document Number	Rev	1A-D581P	
Date	Wednesday, September 07, 2016	Sheet	32	of 80

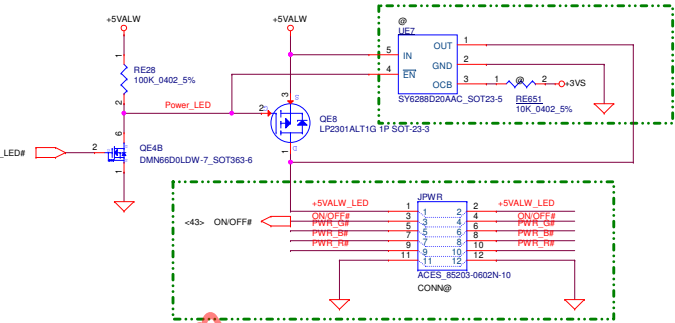
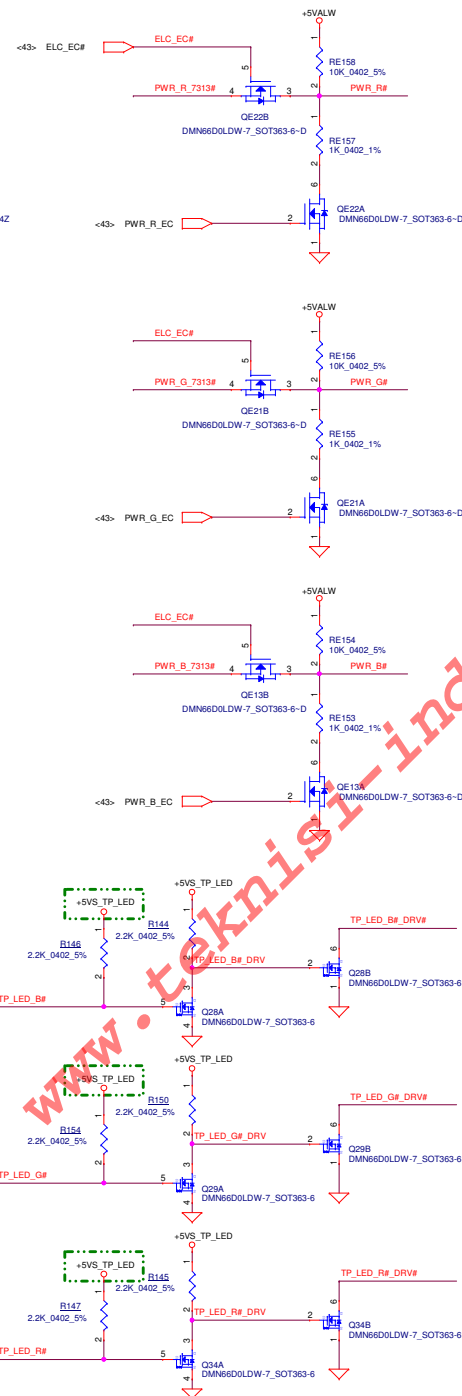
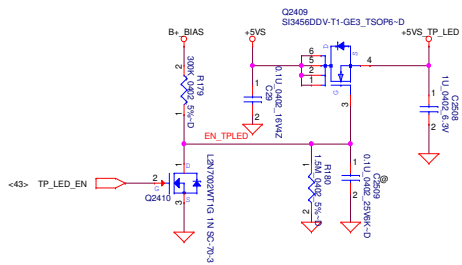




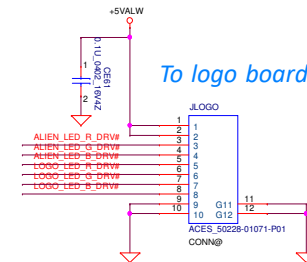
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Issued Date	2015/09/18	Deciphered Date	2016/09/18	Title	ELC (1) C8051F383	
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				Custom	LA-D581P	
Date:				Wednesday, September 07, 2016	Sheet	37 of 80



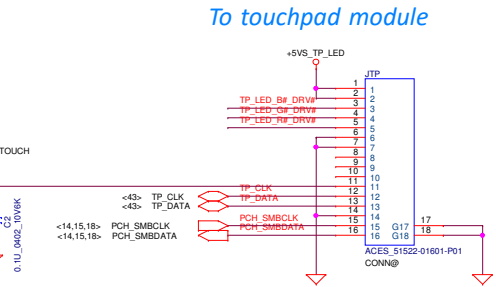
Touchpad LED circuit



To power board



To logo board

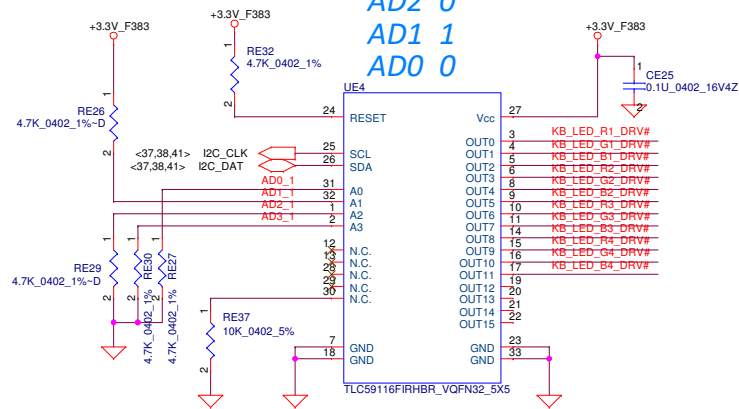


To touchpad module

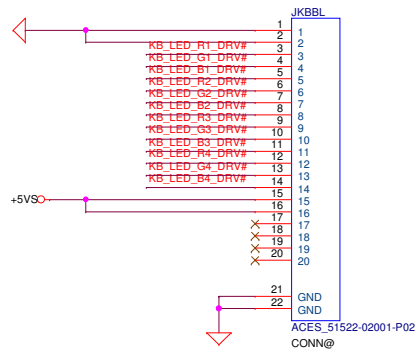
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Deciphered Date	2016/09/18	Title
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Size	Document Number	LA-D581P
Customer	Date	Wednesday, September 07, 2016
Sheet	38	of 80

KB Backlight

AD3 0
AD2 0
AD1 1
AD0 0

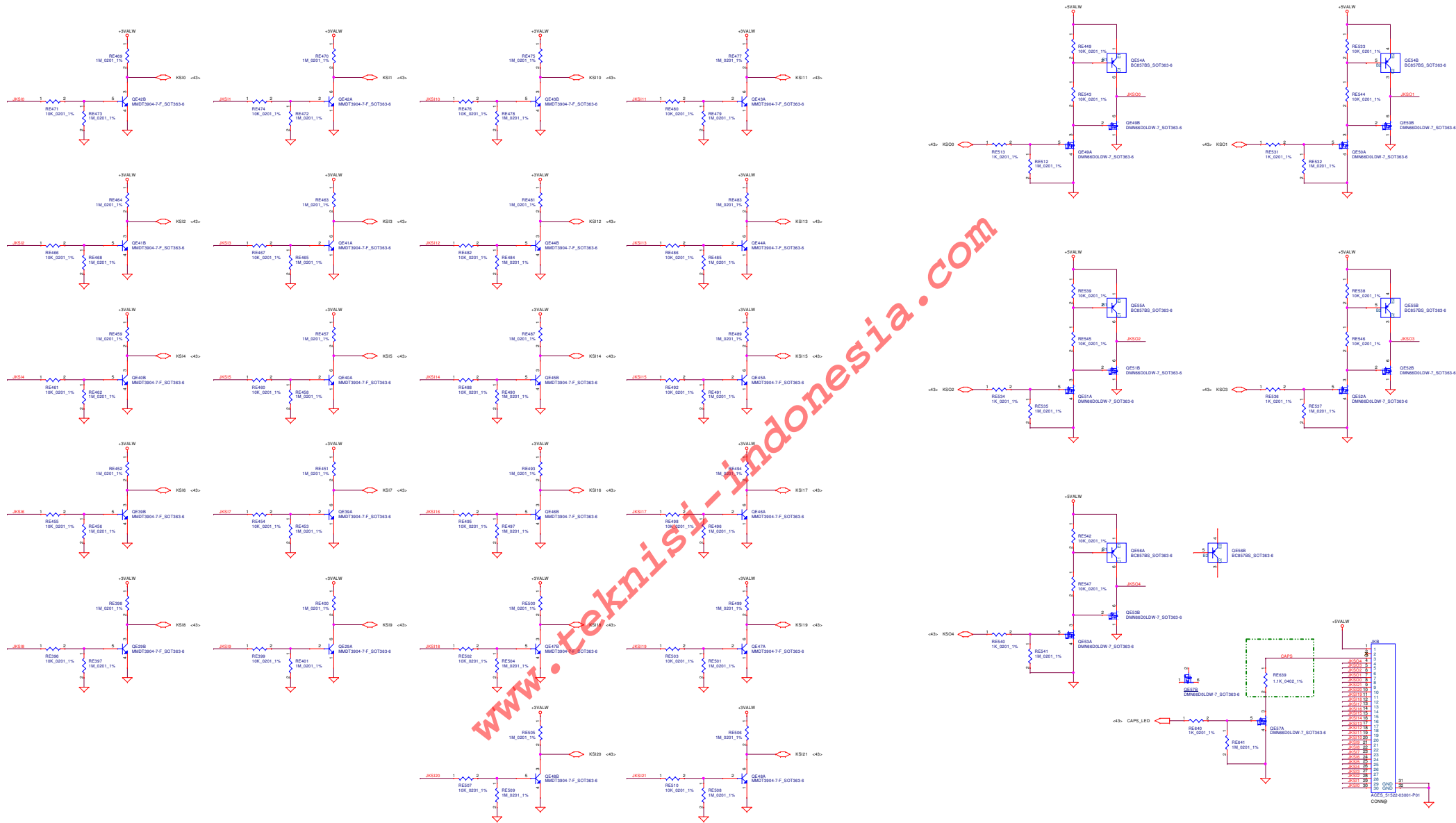


KB BL LED

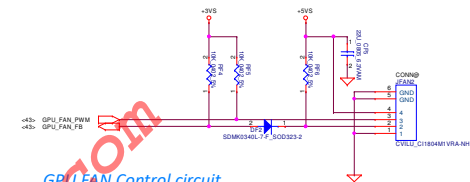
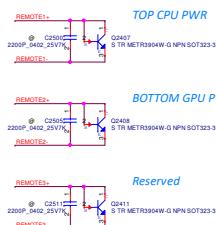
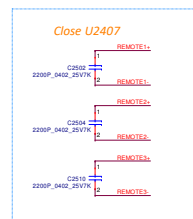
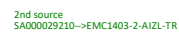


www.teknisi-indonesia.com

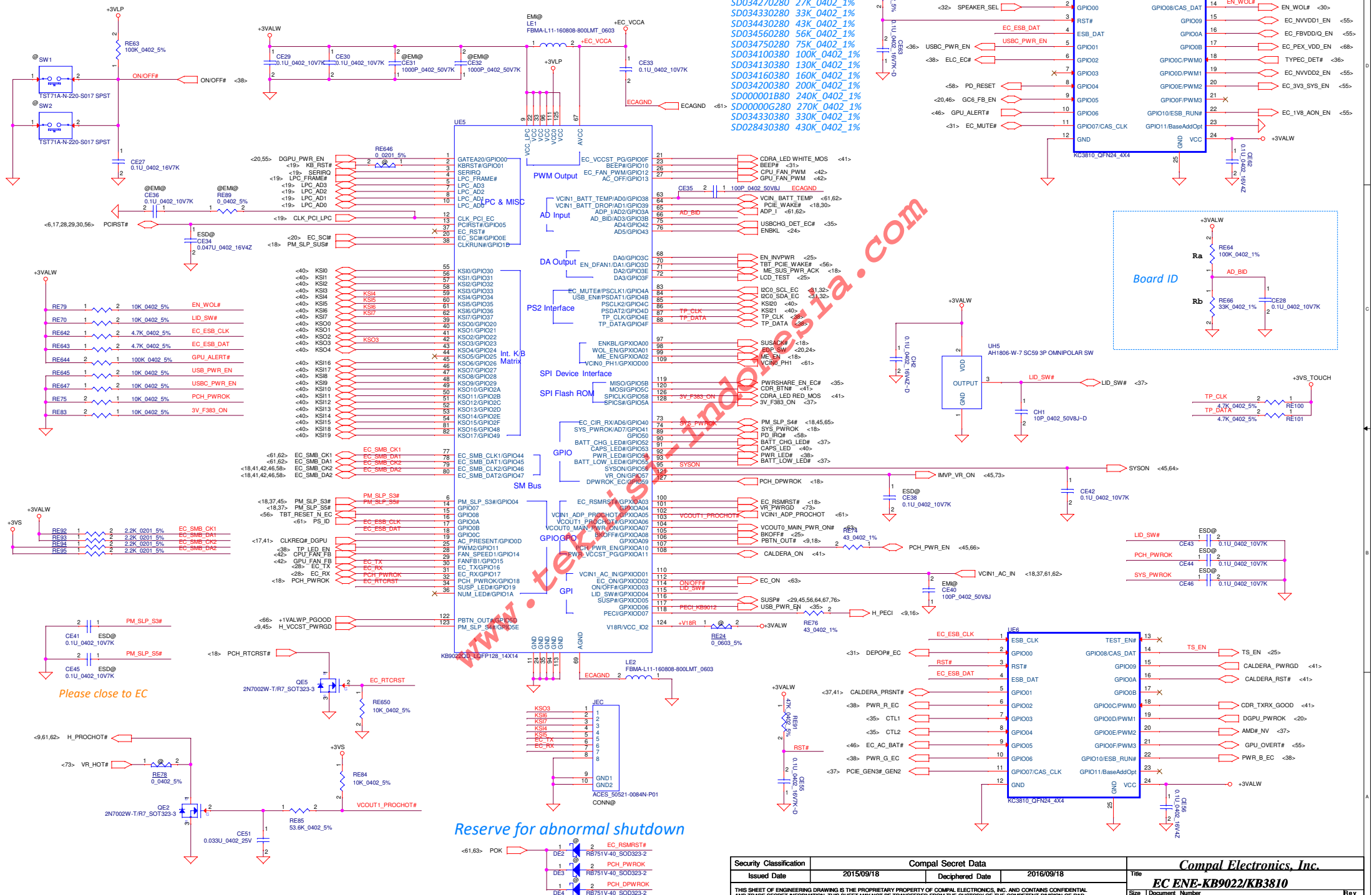
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				Custom	LA-D581P	0.4
				Date: Wednesday, September 07, 2016		
				Sheet 39 of 80		



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Drawn	LA-D58IP	Checked		Rev	64
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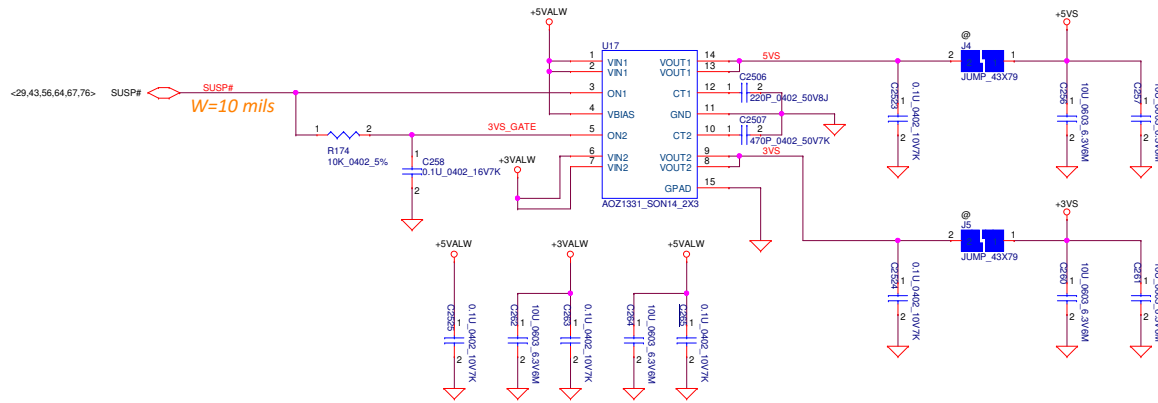


Power ON circuit

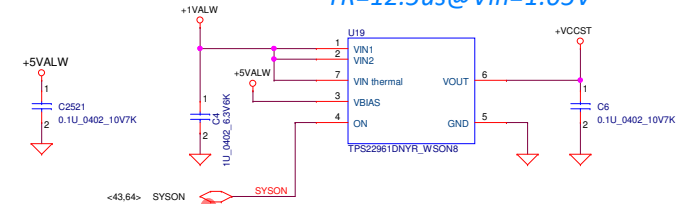


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						Size	Document Number		Rev
						LA-D581P			0.4
						Date:	Wednesday, September 07, 2016	Sheet	43 of 80

20m ohm/6A per channel



+VCCST switch
4.4mohm/6A
TR=12.5us@Vin=1.05V

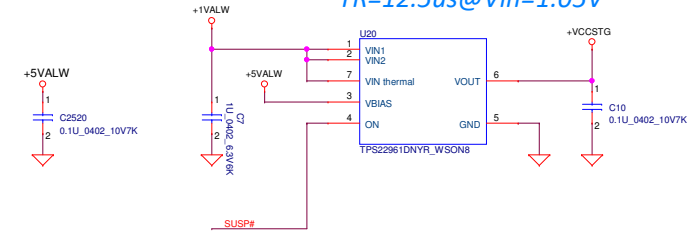


```

Main source  TI SA00007XR00 (SIC TPS22961DN'R V8 ON 8P LOADS W/CH)
2nd source   ACS SA00008A800 (SIC ACZ1334D-01 DF N 8P S NGLS LOADS W/
3rd source   E MC SA00008R600 (SIC E M201V DF NBX3 8P LOADS W/CH)
4st source   APEC SA00006V300 (SIC APE8939GNB DF N 8P LOADS W/CH)

```

+VCCSTG switch
4.4mohm/6A
 $TR=12.5\mu s @ V_{in}=1.05V$

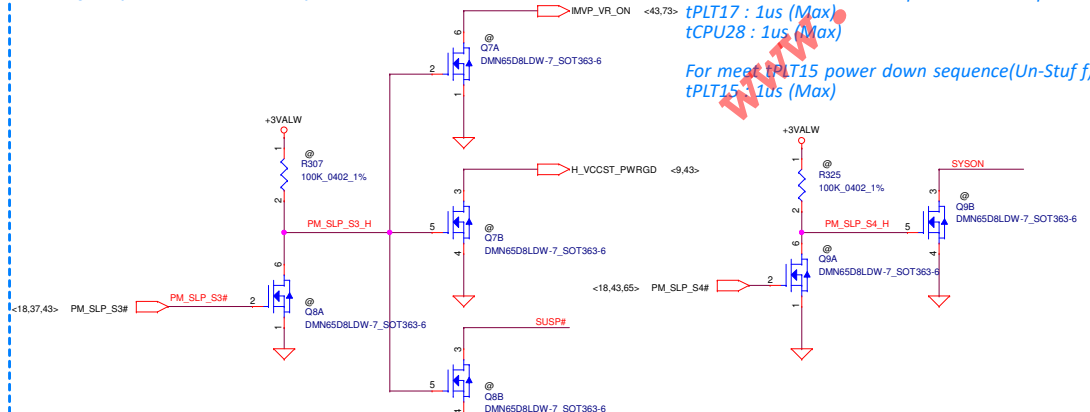


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Main source      TI SA00007XR00 (SIC TPS22961DNR V8 ON 8P LOADS WTC)
2nd source      ACS SA00008A800 (SIC ACZ1334D-01 DFN 8P S NGLE LOADS W
3rd source      E MC SA00008R600 (SIC E MA0201V DF NBX3 8P LOADS WTC)
4th source      APEC SA00006V300 (SIC APE8939GNB DFN 8P LOADS WTC)

```

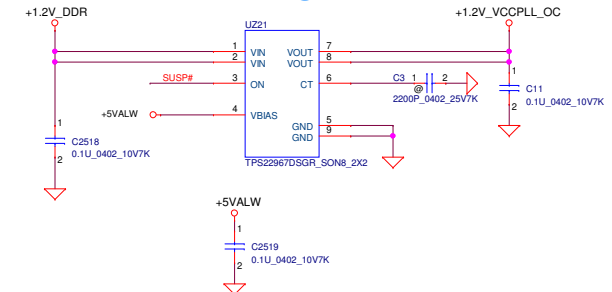
add for power down sequence



For meet tPLT17 & tCPU28 power down sequence.

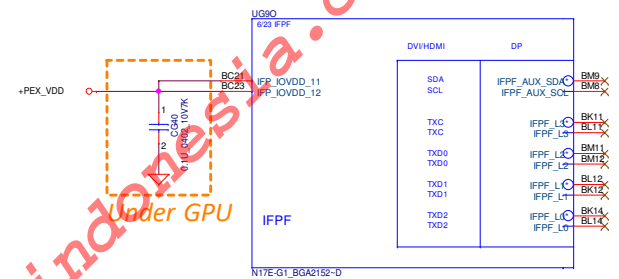
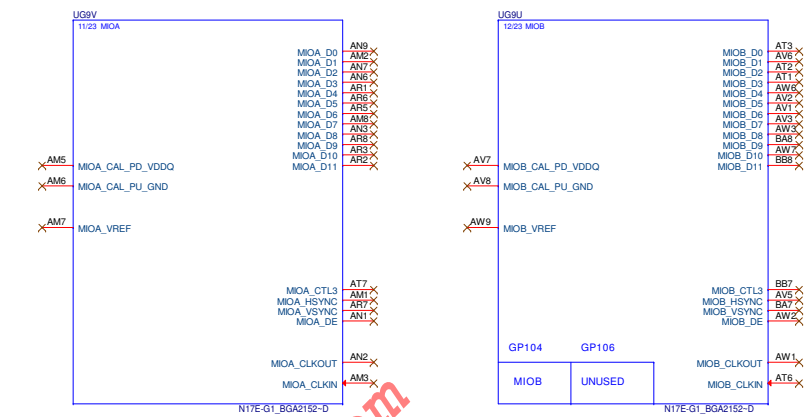
For meet tPLT15 power down sequence(Un-Stuff)
tPLT15 : 1us (Max)

+1.2V_VCCPLL_OC switch
22mohm/4A
TR=520us@Vin=0.8V

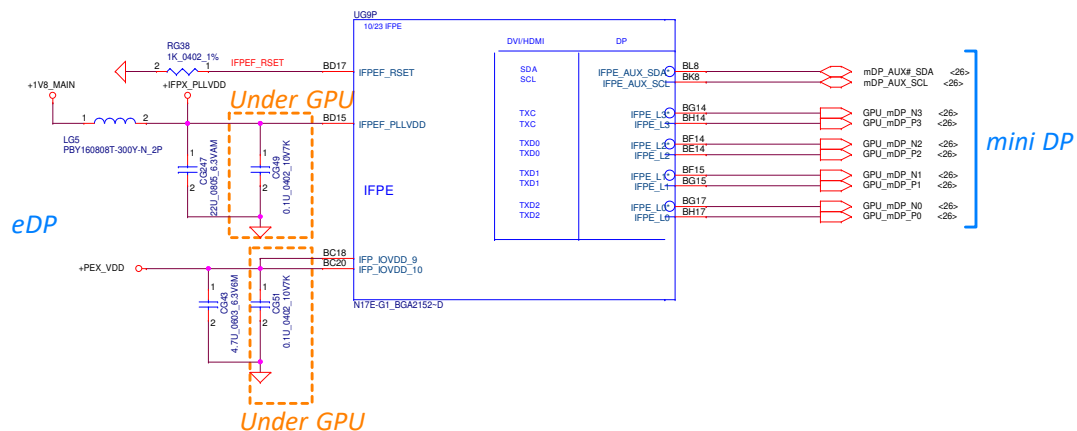


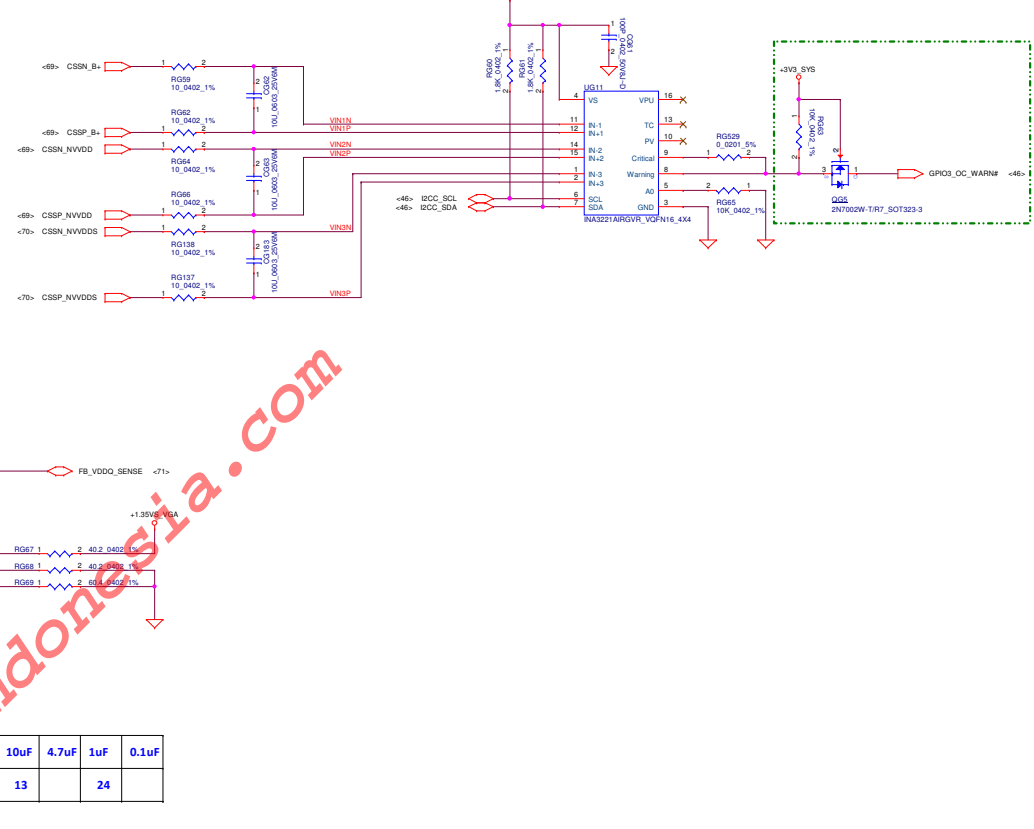
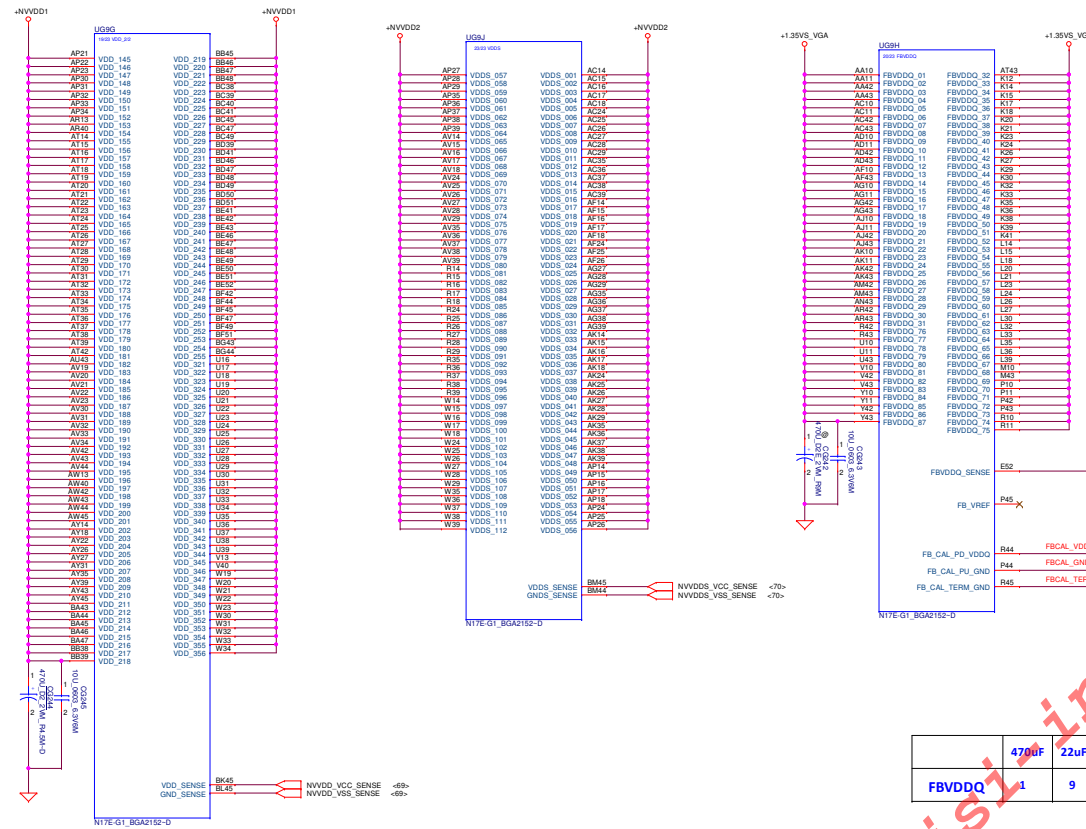
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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				LA-D581P		0.4
Date:				Wednesday, September 07, 2016	Sheet	45 of 80



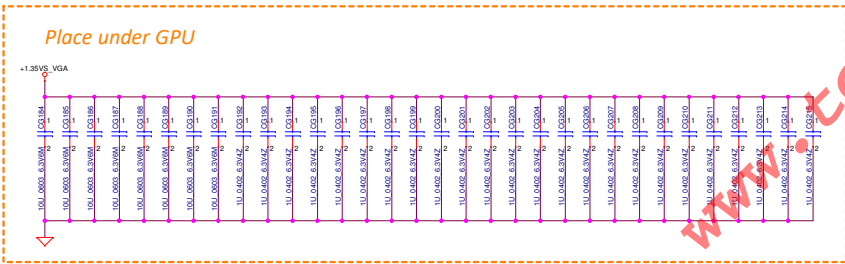


	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			2		4
IFPx_PLLVDD	1				2



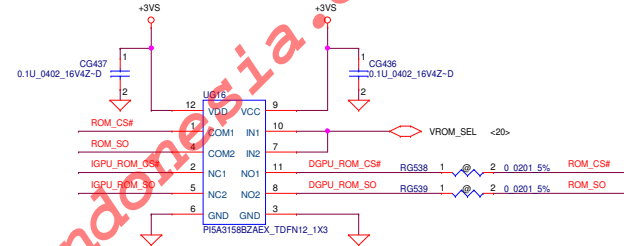
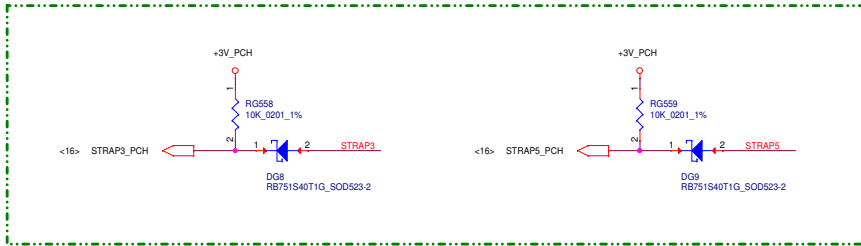
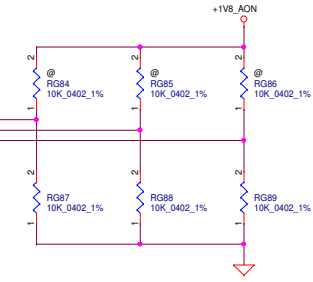
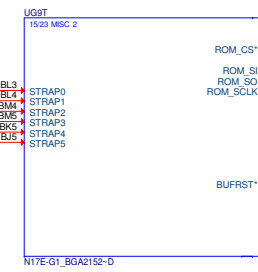
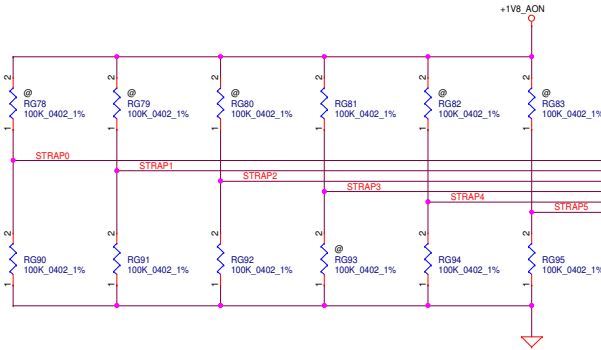


	4700F	22uF	10uF	4.7uF	1uF	0.1uF
FBVDDQ	1	9	13		24	

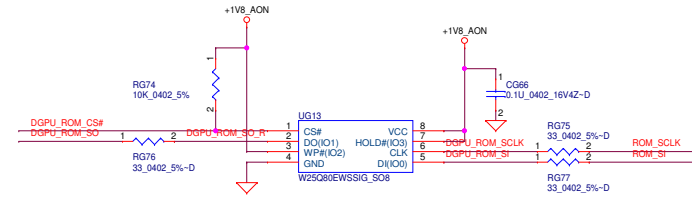
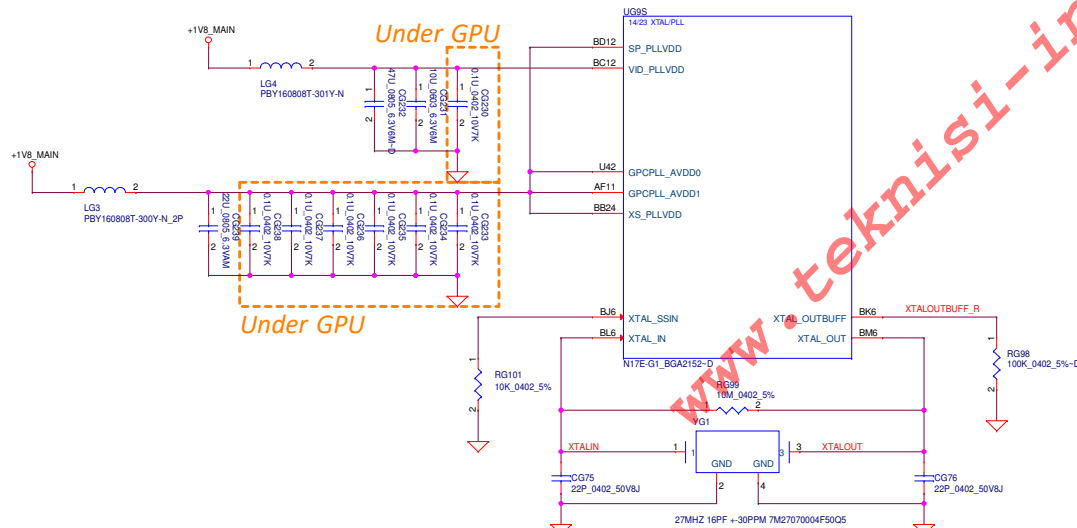


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Size	Document	Number	LA-D581P	
Custom			Rev 0.4	
Date: Wednesday, September 09, 2016				Sheet 49 of 80

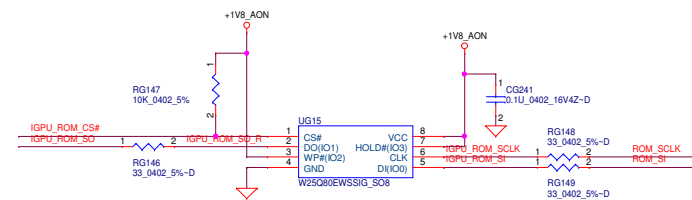
	47uF	22uF	10uF	4.7uF	1uF	0.1uF
VID_PLLVDD	1		1			1
SP_PLLVDD		1				
GPCPLL_AVDD						6



Function	VROM_SEL
COM = NC	L
COM = NO	H



DGPU VBIOS ROM

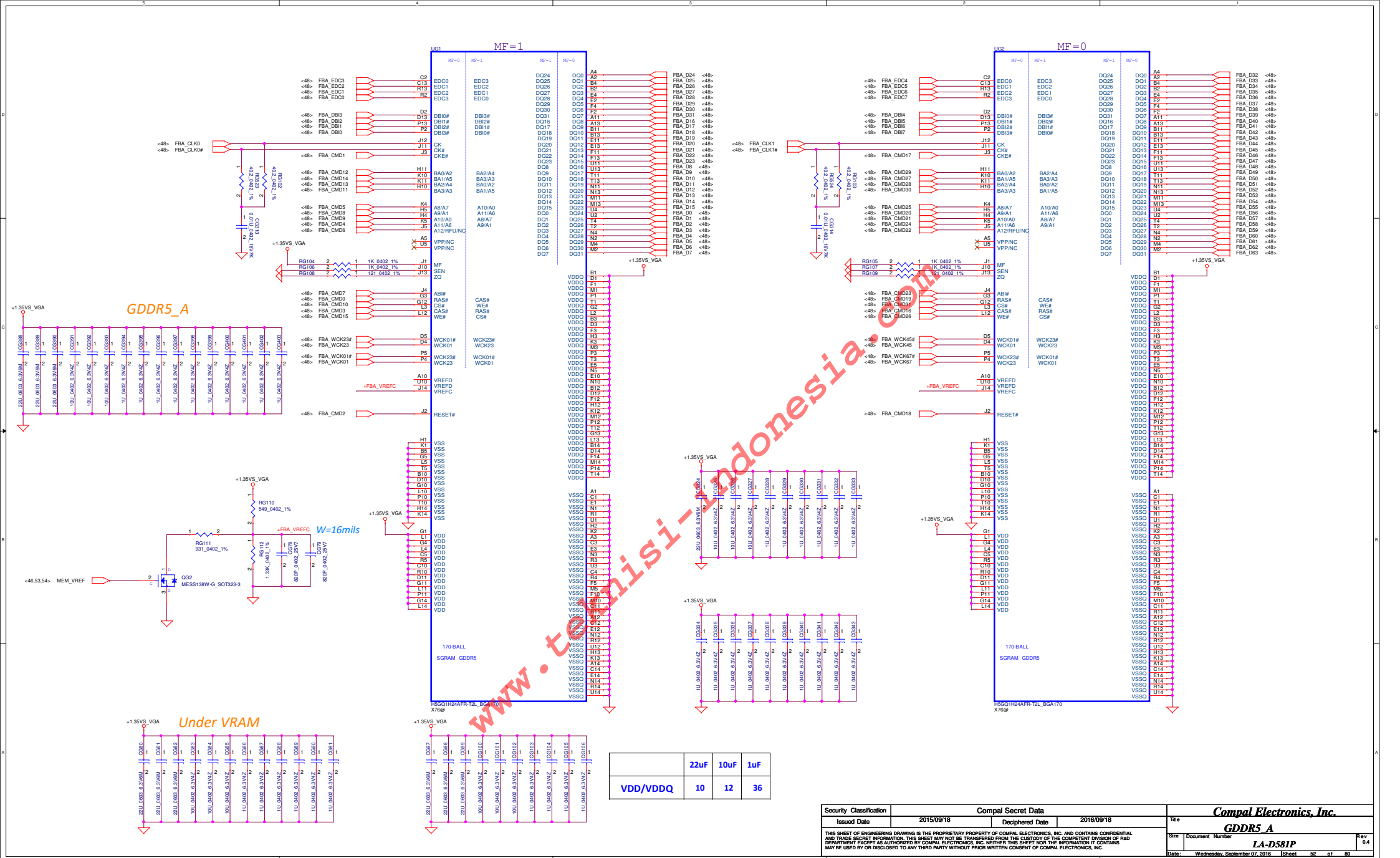


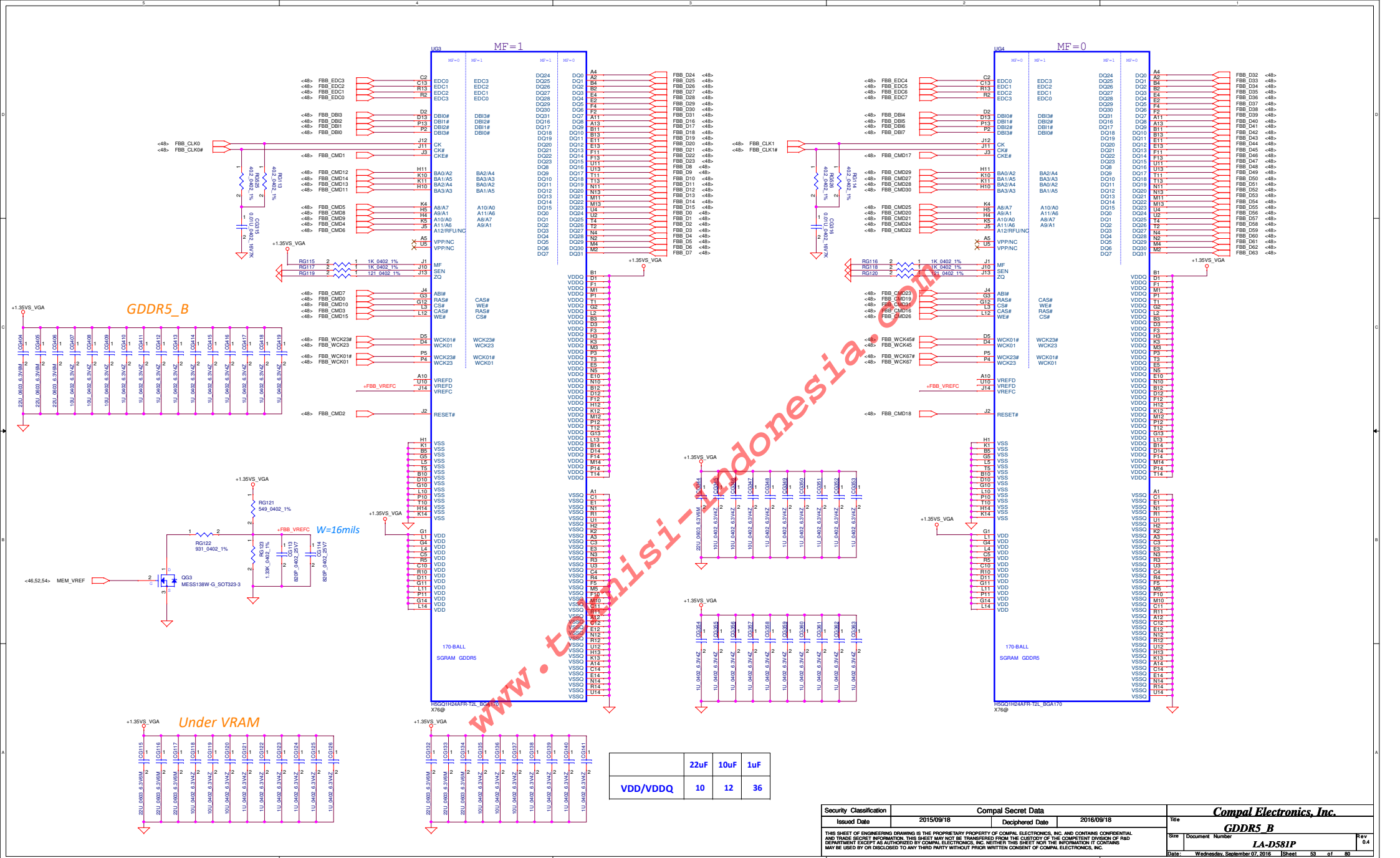
Opti ms VB OS ROM

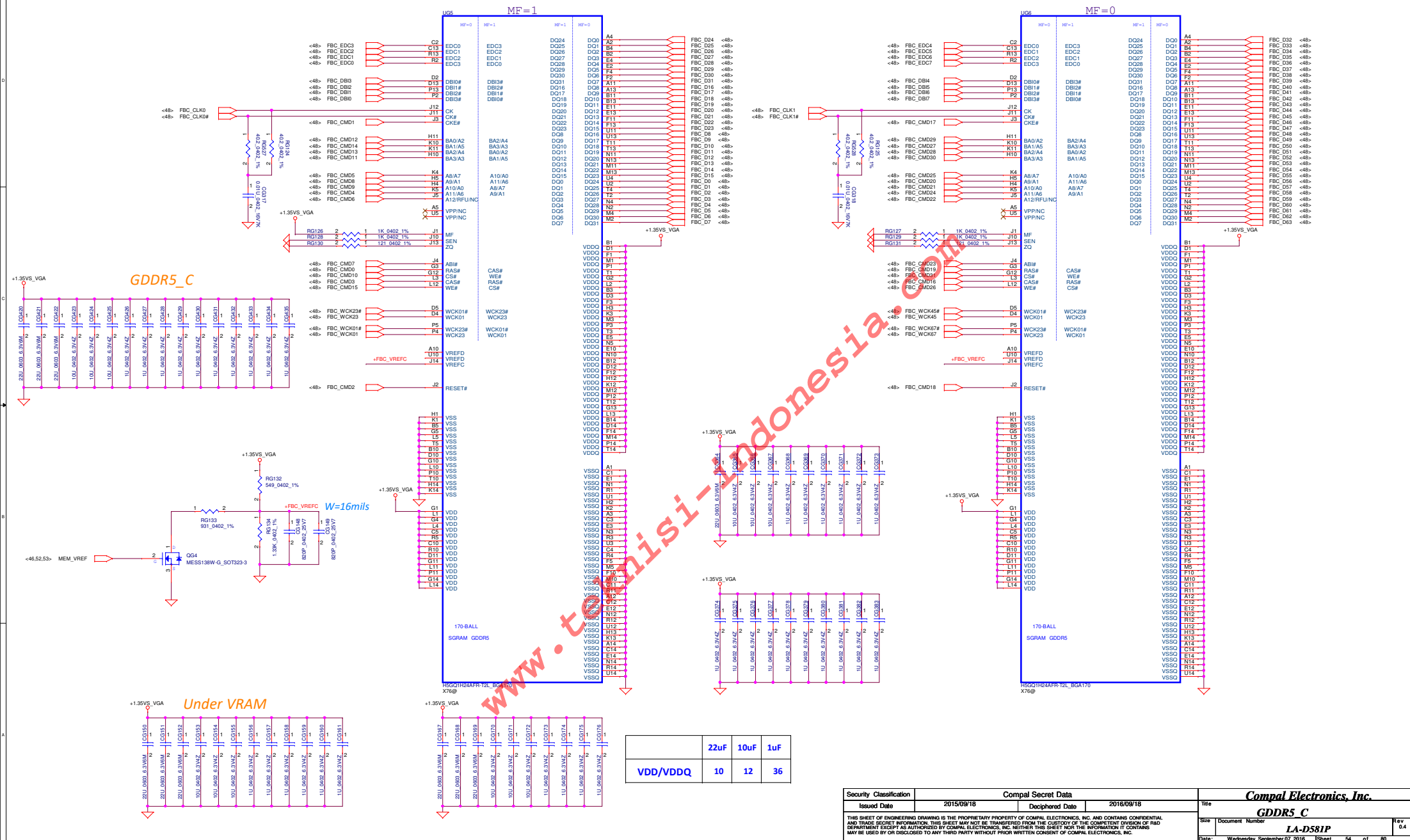
N17E VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
SAMSUNG , K4G80325FB-HC25	L	L	L	H	L	L	0
MICRON , MT51J256M32HF-80:A	H	L	L	H	L	L	1
HYNIX , H5GQ8H24MJR-R4C	L	H	L	H	L	L	2

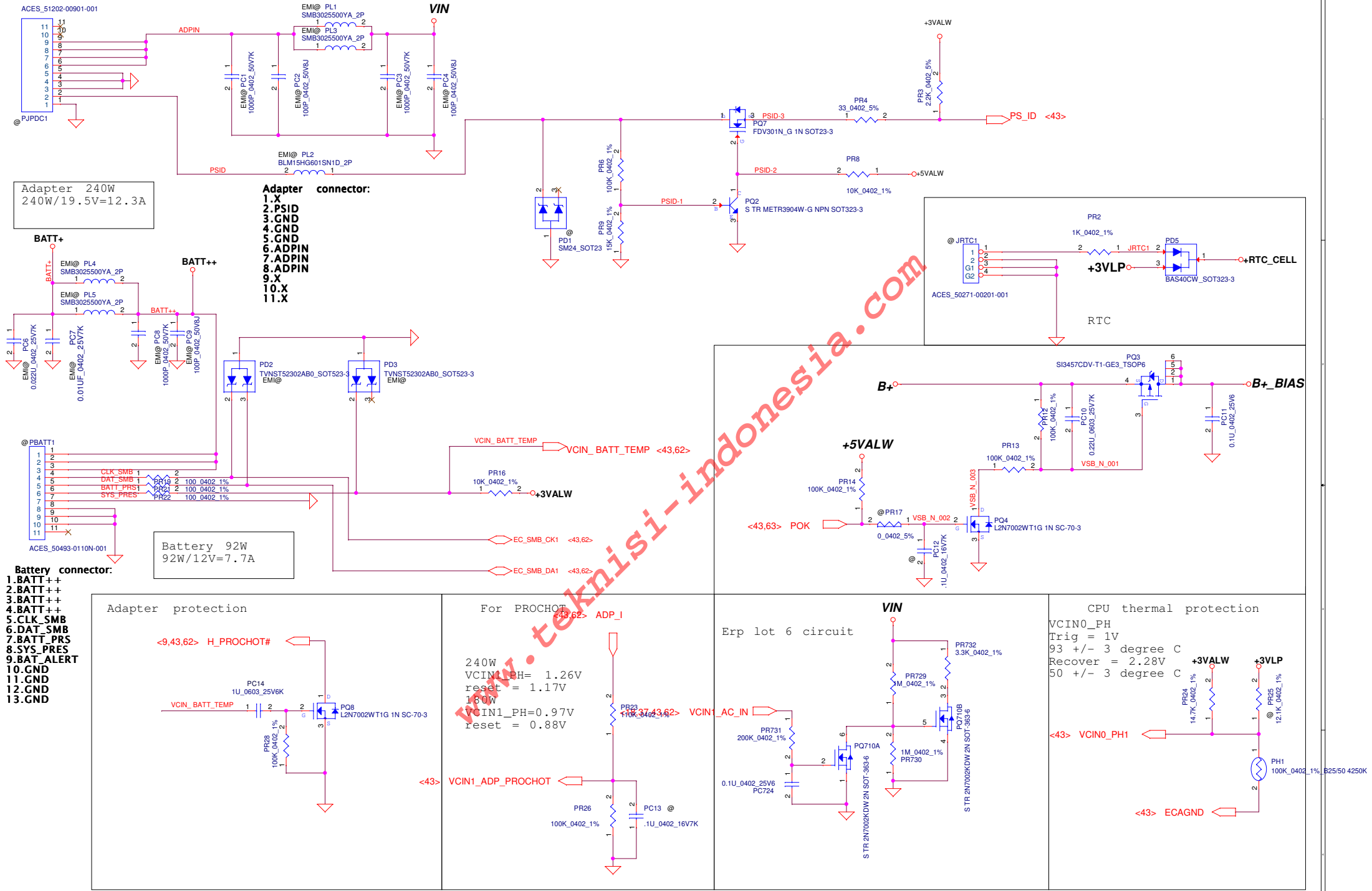
N17P VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
SAMSUNG , K4G80325FB-HC28	L	L	L	H	L	L	0
MICRON , MT51J256M32HF-70:A	H	L	L	H	L	L	1
HYNIX , H5GQ8H24MJR-R0C	L	H	L	H	L	L	2
SAMSUNG , K4G41325FE-HC28	H	H	H	H	L	L	7
HYNIX , H5GC4H24AJR-R0C	L	H	H	H	L	L	6

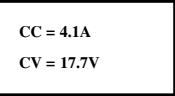
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				Document Number LA-D581P
				Rev 0.4
				Date: Monday, September 26, 2016 Sheet 51 of 80









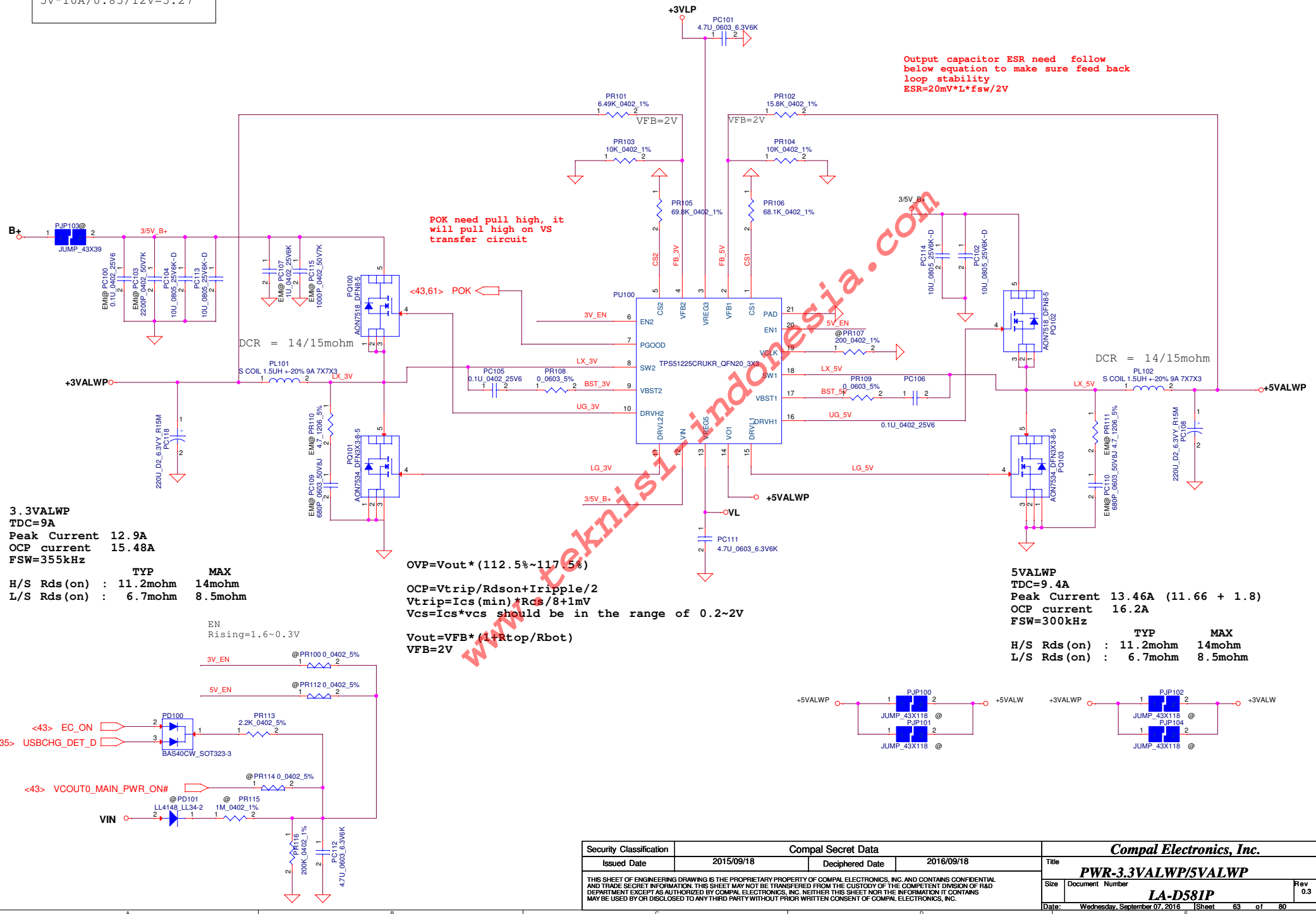


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						Document Number		Rev
						LA-D581P		0.3
Date: Wednesday, September 07, 2016						Sheet 62 of 80		

Input Current: 7.5A
 $3.3V \times 10A / 0.85 / 12V = 2.23$
 $5V \times 10A / 0.85 / 12V = 5.27$

Output capacitor ESR need follow
below equation to make sure feed back
loop stability
 $ESR = 20mV \times L \times f_{sw} / 2V$

POK need pull high, it
will pull high on VS
transfer circuit



3.3VALWP
TDC=9A
Peak Current 12.9A
OCP current 15.48A
FSW=355kHz

TYP
H/S Rds(on) : 11.2mohm
L/S Rds(on) : 6.7mohm

MAX
14mohm
8.5mohm

EN
Rising=1.6~0.3V

$OVP = V_{out} \times (112.5\% \sim 117.5\%)$
 $OCP = V_{trip} / R_{dson} + I_{ripple} / 2$
 $V_{trip} = I_{cs}(\min) \times R_{cs} / 8 + 1mV$
 $V_{cs} = I_{cs} \times v_{cs}$ should be in the range of 0.2~2V
 $V_{out} = V_{FB} \times (1 + R_{top} / R_{bot})$
VFB=2V

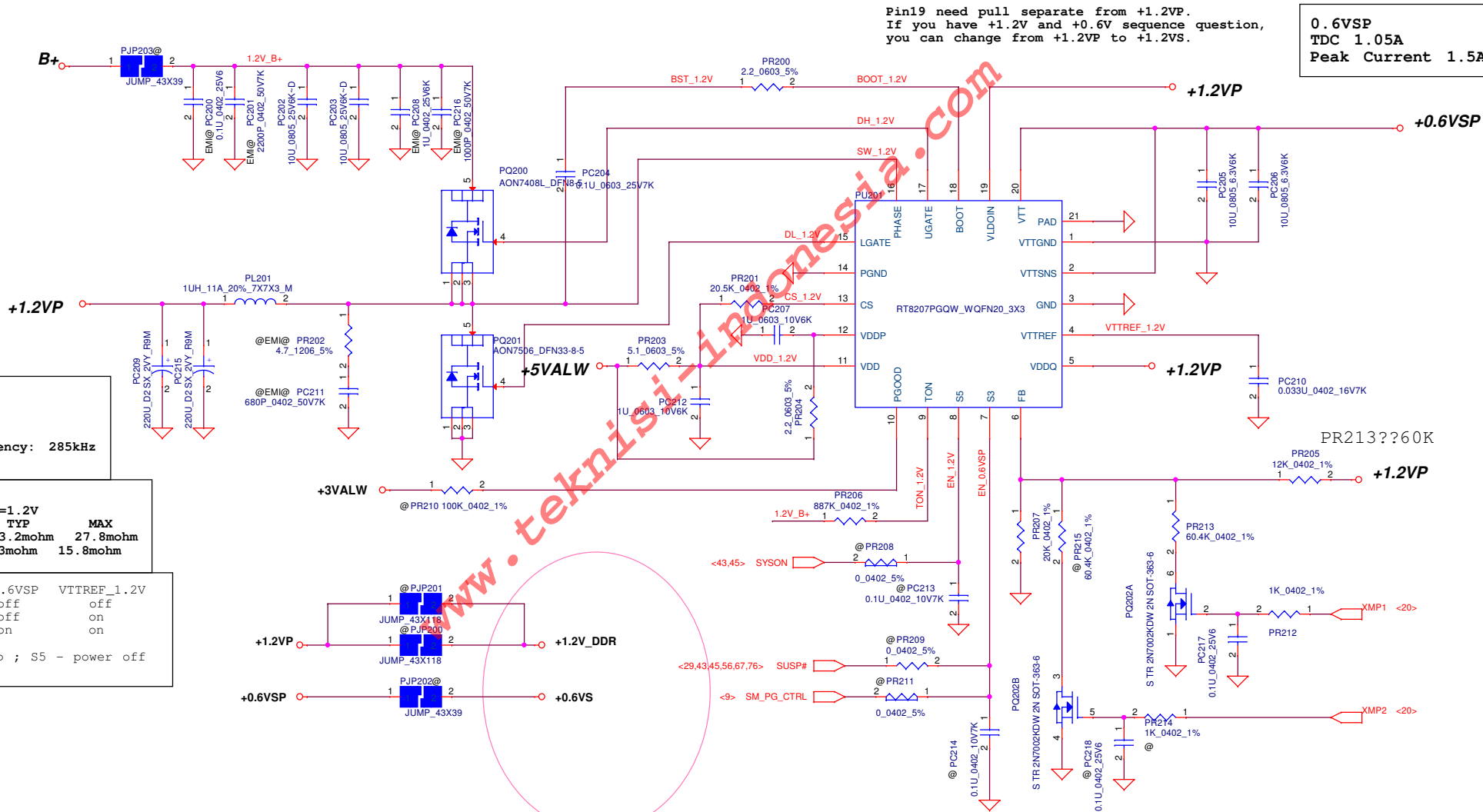
5VALWP
TDC=9.4A
Peak Current 13.46A (11.66 + 1.8)
OCP current 16.2A
FSW=300kHz

TYP
H/S Rds(on) : 11.2mohm
L/S Rds(on) : 6.7mohm

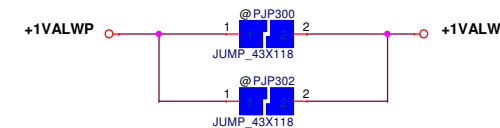
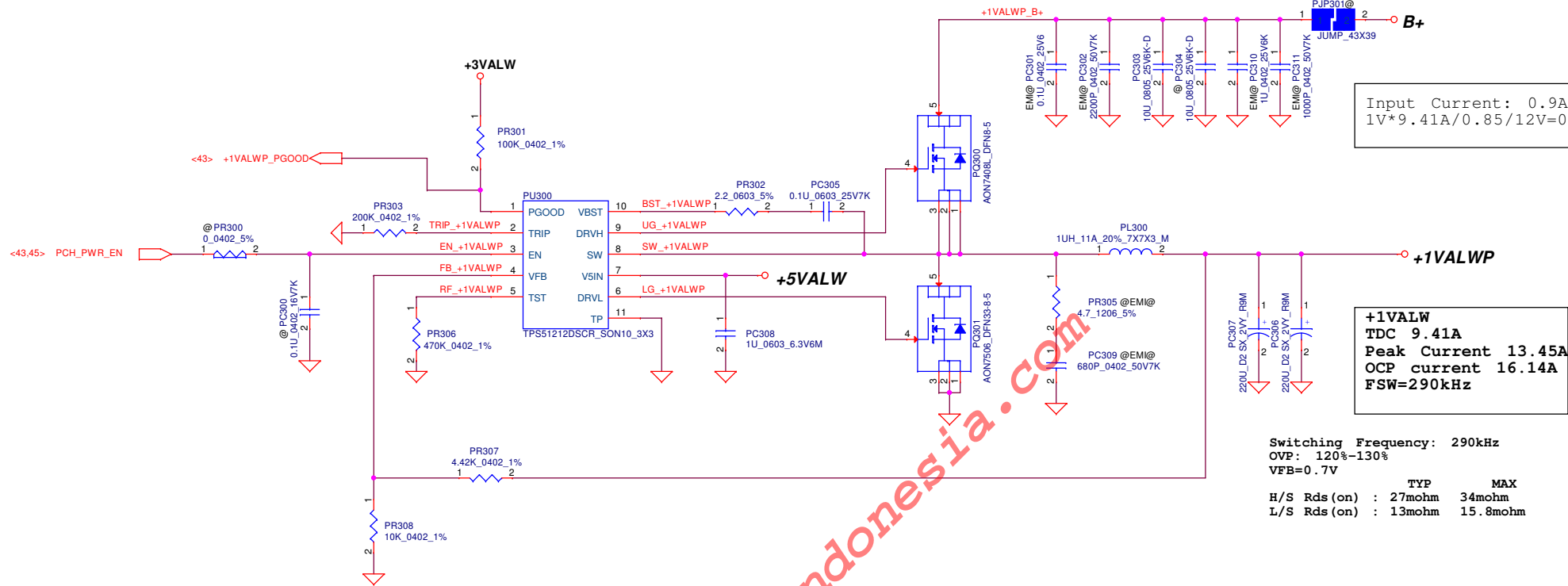
MAX
14mohm
8.5mohm

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				LA-D581P	
				Date	Wednesday, September 07, 2016
				Sheet	63 of 80

Input Current: 1A
 $1.2V \times 8.88A / 0.85 / 12V = 1$

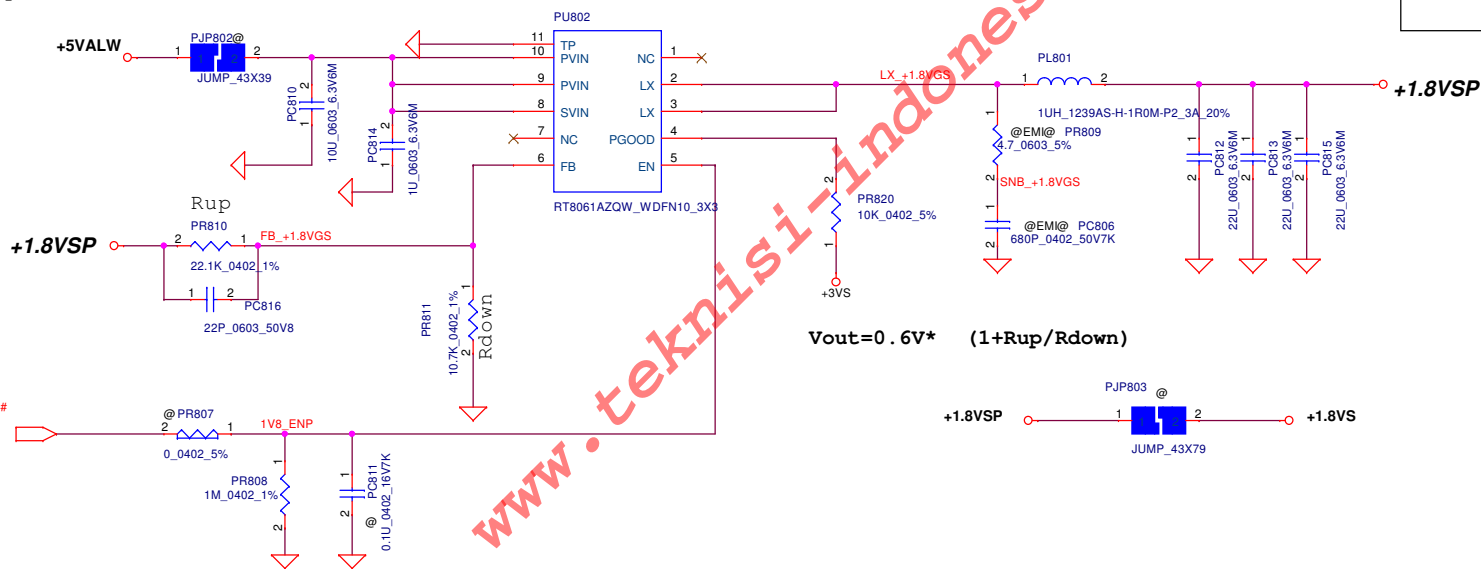


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Size	Document Number	Rev		LA-D581P	
Date:		Wednesday, September 07, 2016		Sheet	64 of 80



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2015/09/18		Deciphered Date		2016/09/18		Title	
										PWR-+1VALWP	
										LA-D581P	
										Rev 0.3	
										Date: Wednesday, September 07, 2016	
										Sheet 66 of 80	

Input 0.4A



+1.8VSP
TDC 2.26A
Peak Current 3A
OCP current 4A
FSW=1MHz
Choke DCR TYP MAX
0.045mohm , 0.059mohm

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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										PWR +1.8VSP/+1.8VGSP	
										LA-D581P	
										Rev 0.3	
										Date: Wednesday, September 07, 2016	
										Sheet 67 of 80	

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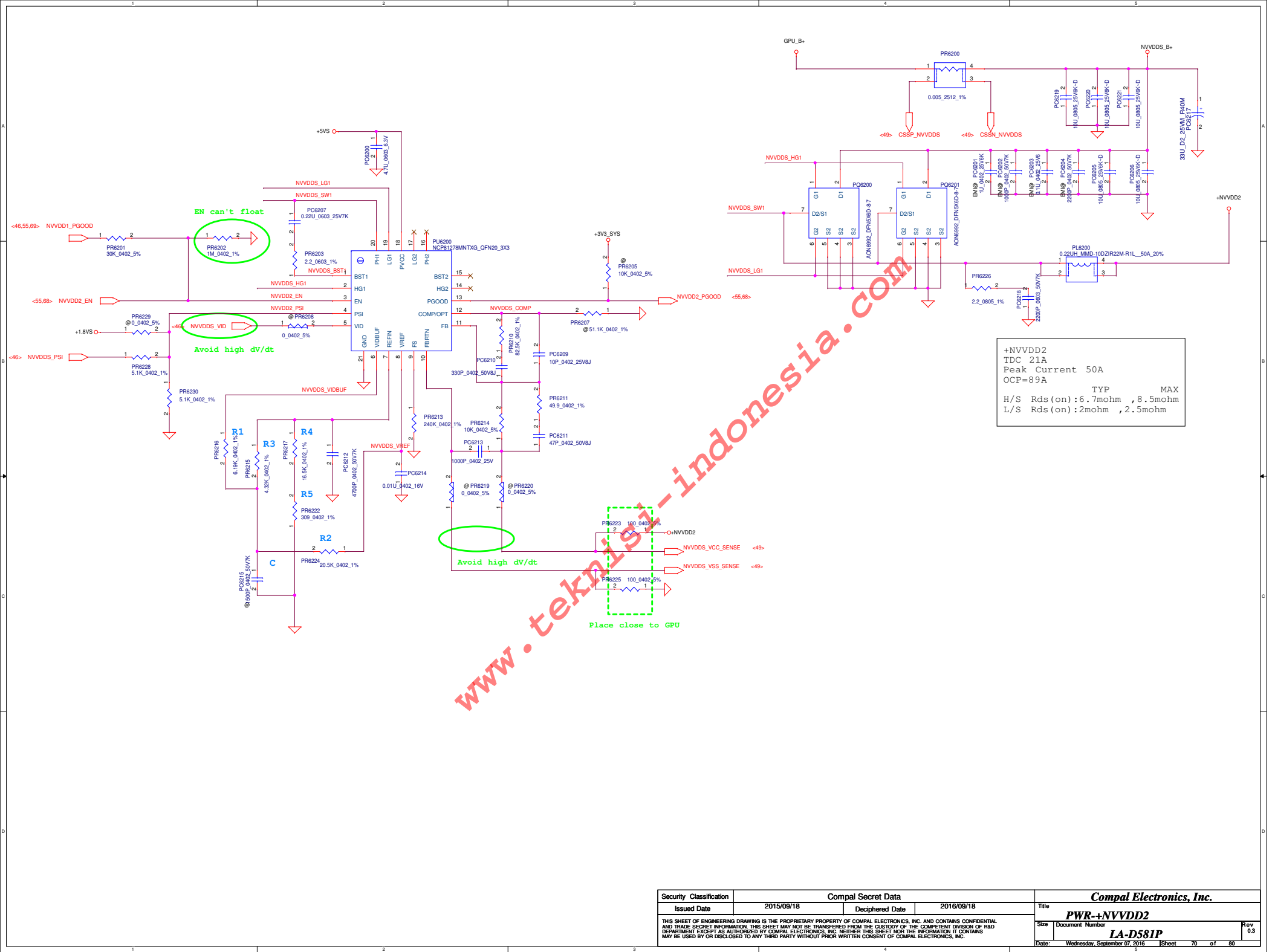
Input 0.7A

+1.0VS_VGAP
TDC 3A
Peak Current 3A
OCP current 6A
FSW=1MHz

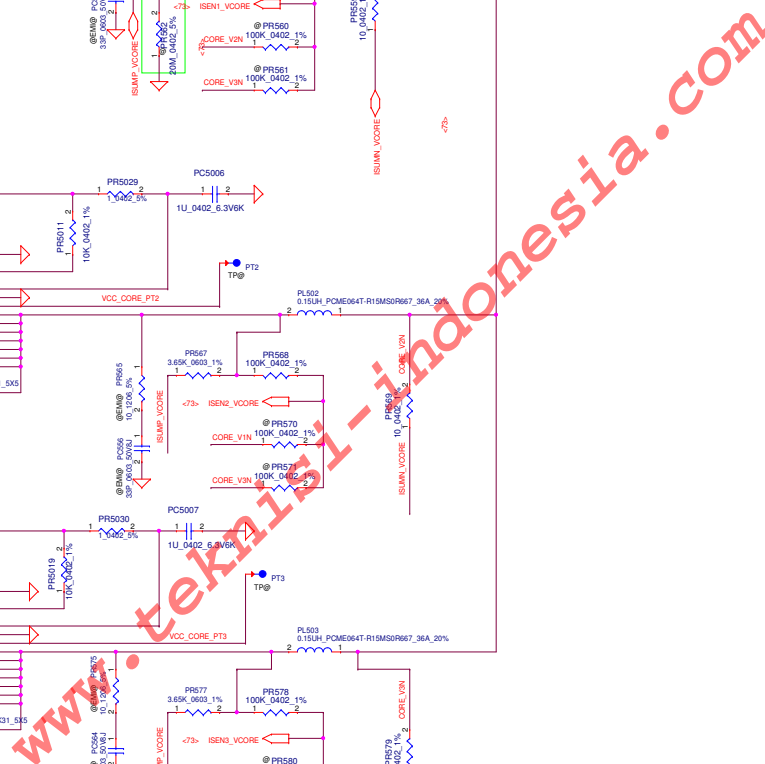
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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Size	Document Number	Rev		LA-D581P	
Date: Wednesday, September 07, 2016		Sheet		68 of 80	
				0.3	

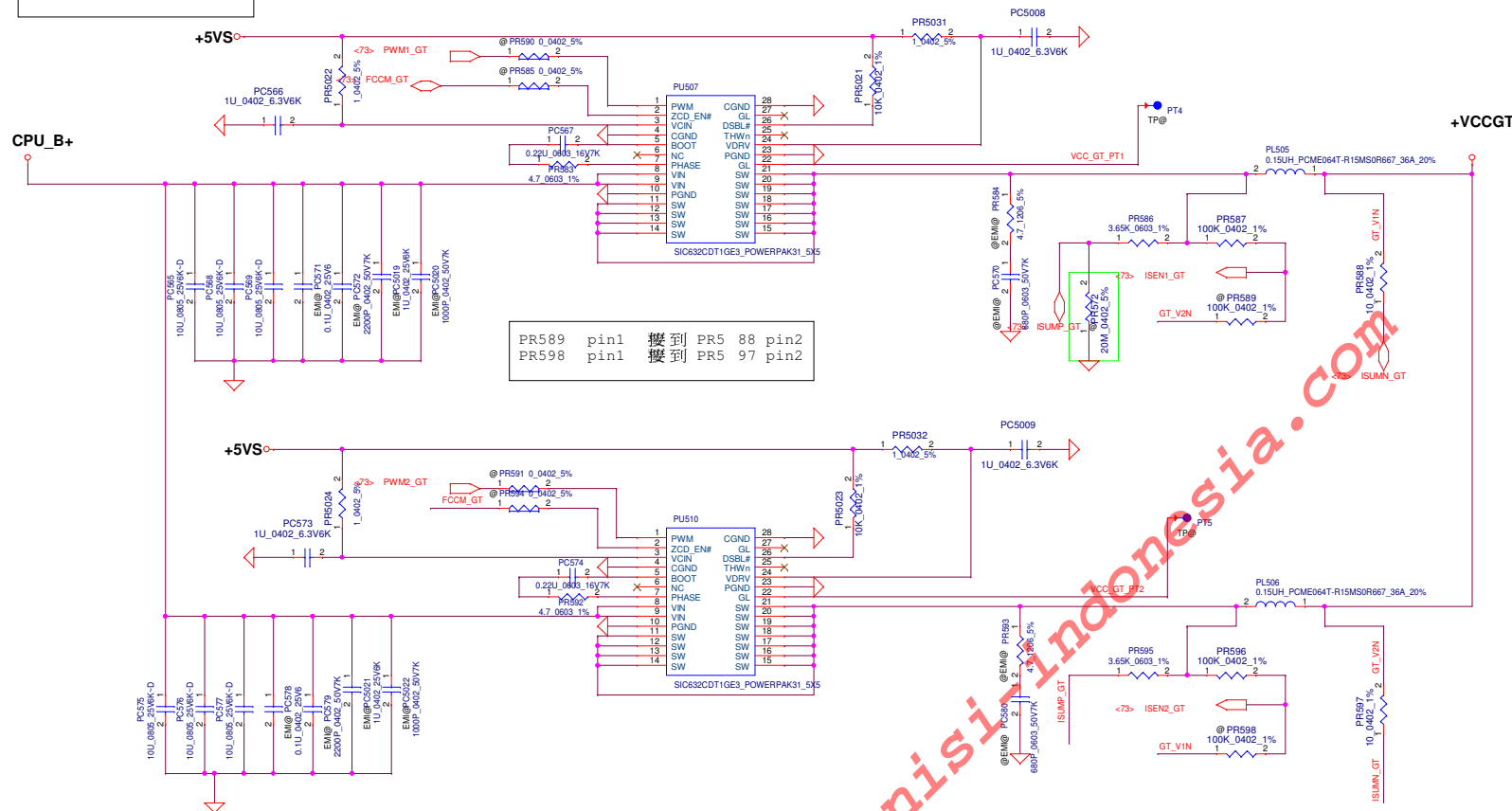


VCC_CORE
TDC_PL2 :56A
Peak Current 68A
OCP Current 81.6A
DCR 0.66mohm +/-7%
Load Line 1.8mV/A



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				Sheet	74 of 80	
				Date:	Wednesday, September 23, 2016	Sheet

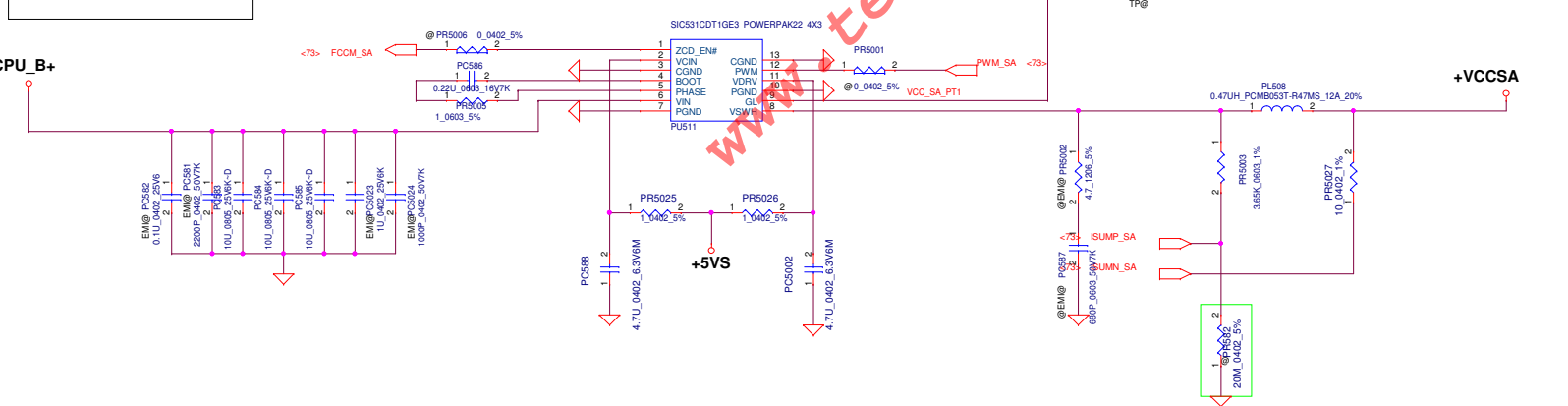
Input Current: 5.7A
1.5V*39A/0.85/12V=5.7



VCC_GT
TDC PL2 :39A
Peak Current 54A
OCP Current 64.8A
DCR 0.66mohm +/-7%
Load Line 2.65mV/A

PR589 pin1 接到 PR5 88 pin2
PR598 pin1 接到 PR5 97 pin2

Input Current: 1.0A
1.05V*10A/0.85/12V=1.0



VCC_SA
TDC PL2 :10A
Peak Current 11A
OCP Current 13.2A
DCR 7.4mohm typ
Load Line 9.1mV/A

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Size	Document Number	LA-D581P		Rev 0.4
Date:	Wednesday, September 07, 2016	ISheet	75	of 80

+VCC_CORE

+VCCGT

+VCCSA

VCC_CORE	
220uF X3	
47uF_0805 X 4	
22uF_0603 X 8	
10uF_0402 X 28	
1uF_0201 X 63	

VCC_GT	
220uF X4	
47uF_0805 X 6	
22uF_0603 X 8	
10uF_0402 X 3	
1uF_0201 X 68	

VCC_SA	
220uF X1	
47uF_0805 X 1	
10uF_0402 X 7	
1uF_0201 X 3	

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				PWR_CPU DECOUPLING	
				IA-D581P	
				Rev	0.3
				Date	Wednesday, September 07, 2016
				Sheet	77 of 80